ORIGINAL

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U.S. DISTRICT COURT
NORTHERN DISTRICT OF TEXAS
FILED
JUN - 9 2008
CLERK, U.S. DISTRICT COURT
By RR
Deputy

IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF TEXAS
DALLAS DIVISION

FAST MEMORY ERASE, LLC *Plaintiff,* vs. SPANSION, INC., SPANSION LLC, INTEL CORPORATION, NUMONYX B.V., NUMONYX, INC., STMICROELECTRONICS NV, STMICROELECTRONICS, INC., NOKIA CORPORATION, NOKIA INC., SONY ERICSSON MOBILE COMMUNICATIONS AB, SONY ERICSSON MOBILE COMMUNICATIONS (USA), INC. and MOTOROLA, INC. *Defendants.*	CIVIL CASE NO. ________________ **3-08CV0977-M** **JURY TRIAL DEMANDED** 22599

FAST MEMORY ERASE, LLC'S ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT AND JURY DEMAND

Plaintiff Fast Memory Erase LLC ("Fast Erase") files this Complaint for patent infringement against Defendants Spansion, Inc. and Spansion LLC ("Spansion"); Intel Corporation ("Intel"); Numonyx B.V. and Numonyx, Inc. (collectively, "Numonyx"); STMicroelectronics NV and STMicroelectronics, Inc. (collectively "STMicro") Nokia Corporation and Nokia, Inc. (collectively, "Nokia"); Sony Ericsson Mobile Communications AB and Sony Ericsson Mobile Communications (USA), Inc. (collectively, "Sony Ericsson") and Motorola, Inc. ("Motorola") (collectively, the "Defendants") and alleges as follows:

I. PARTIES

1. Fast Erase is a Texas corporation having its principal place of business at 15455 Dallas Parkway, 6th Floor, Addison, Texas 75001.

2. Upon information and belief, Spansion, Inc. is a Delaware corporation having its principal place of business at 915 Deguigne Drive, Post Office Box 3453, Sunnyvale, California 94088. Upon information and belief Spansion, Inc. is authorized to do business in Texas and may be served with process by serving its registered agent CT Corporation System, 350 N. St. Paul Street, Suite 2900, Dallas, Texas 75201.

3. Upon information and belief, Spansion LLC is a Delaware corporation having its principal place of business at 915 Deguigne Drive, Post Office Box 3453, Sunnyvale, California 94088. Upon information and belief, Spansion LLC is authorized to do business in Texas and may be served with process by serving its registered agent CT Corporation System, 350 N. St. Paul Street, Suite 2900, Dallas, Texas 75201.

4. Upon information and belief, Intel Corporation is a California corporation having its principal place of business at 2200 Mission College Blvd., Santa Clara, CA 95054. Upon information and belief, Intel is authorized to do business in Texas and may be served with process by serving its registered agent CT Corporation System, 350 N. St. Paul Street, Suite 2900, Dallas, Texas 75201.

5. Upon information and belief, Numonyx B.V. is a Swiss corporation having its principal place of business at A-One Biz Center, Z.A. Vers la Piece, Rte de l'Etraz, 1180 Rolle, Switzerland. Upon information and belief, Numonyx B.V. is a nonresident of Texas who engages in business in this state, but does not maintain a regular place of business in this state or a designated agent for service of process in this state. This proceeding arises, in part, out of business done in this state. Upon information and belief, Numonyx B.V. resides in this

jurisdiction within the meaning of 28 U.S.C. § 1400(b). Numonyx B.V. may be served with process in Switzerland pursuant to the Hague Convention on the Service Abroad of Judicial and Extrajudicial Documents.

6. Upon information and belief, Numonyx, Inc. is a Delaware corporation having its principal place of business at 1310 Electronics Drive, Carrollton, Texas 75006. Upon information and belief, Numonyx, Inc. is authorized to do business in Texas and may be served with process by serving its registered agent Corporation Service Company, 2711 Centerville Road, Suite 400 Wilmington, DE 19808.

7. Upon information and belief, STMicroelectronics NV is a Swiss corporation having its principal place of business at 39 Chemin du Champ des Filles, C. P. 21, CH 1228 Plan-Les-Ouates, Geneva, Switzerland. Upon information and belief, STMicroelectronics NV is a nonresident of Texas who engages in business in this state, but does not maintain a regular place of business in this state or a designated agent for service of process in this state. This proceeding arises, in part, out of business done in this state. Upon information and belief, STMicroelectronics NV resides in this jurisdiction within the meaning of 28 U.S.C. § 1400(b). Defendant may be served with process in Switzerland pursuant to the Hague Convention on the Service Abroad of Judicial and Extrajudicial Documents.

8. Upon information and belief, STMicroelectronics, Inc. is a Delaware corporation having its principal place of business at 1310 Electronics Drive, Carrollton, Texas 75006. Upon information and belief, STMicroelectronics, Inc. is authorized to do business in Texas and may be served with process by serving its registered agent Corporation Service Company, 2711 Centerville Road, Suite 400, Wilmington, DE 19808.

9. Upon information and belief, Nokia Corporation is a Finnish corporation having

its principal place of business at Keilalahdentie 2-4, FI-02150 Espoo, Finland. Upon information and belief, Nokia Corporation is a nonresident of Texas who engages in business in this state, but does not maintain a regular place of business in this state or a designated agent for service of process in this state. Upon information and belief, Nokia Corporation resides in this jurisdiction within the meaning of 28 U.S.C. § 1400(b). This proceeding arises, in part, out of business done in this state. Nokia Corporation may be served with process in Finland pursuant to the Hague Convention on the Service Abroad of Judicial and Extrajudicial Documents.

10. Upon information and belief, Nokia, Inc. is a Delaware corporation having its principal place of business at 6000 Connection Drive, Irving, Texas 75039. Upon information and belief, Nokia, Inc. is authorized to do business in Texas and may be served with process by serving its registered agent, National Registered Agents, Inc., 16055 Space Center, Suite 235, Houston, TX 77062.

11. Upon information and belief, Sony Ericsson Mobile Communications AB is a Swedish corporation having its principal place of business at Nya Vattentornet, SE-221 88 Lund, Sweden. Upon information and belief, Sony Ericsson Mobile Communications AB is a nonresident of Texas who engages in business in this state, but does not maintain a regular place of business in this state or a designated agent for service of process in this state. Upon information and belief, Sony Ericsson Mobile Communications AB resides in this jurisdiction within the meaning of 28 U.S.C. § 1400(b). This proceeding arises, in part, out of business done in this state. Sony Ericsson Mobile Communications AB may be served with process in Sweden pursuant to the Hague Convention on the Service Abroad of Judicial and Extrajudicial Documents.

12. Upon information and belief, Sony Ericsson Mobile Communications (USA), Inc.

is a Delaware corporation having its principal place of business at 7001 Development Drive, Research Triangle Park, North Carolina 27709. Upon information and belief, Sony Ericsson Mobile Communications (USA), Inc. is authorized to do business in Texas and may be served with process by serving its registered agent, Capitol Corporate Services, Inc., 800 Brazos, Suite 400, Austin, TX 78701.

13. Upon information and belief, Motorola is a Delaware corporation having its principal place of business at 1303 E. Algonquin Rd., Schaumburg, IL 60196. Upon information and belief, Motorola is authorized to do business in Texas and may be served with process by serving its registered agent, CT Corporation System, 350 N. St. Paul Street, Ste. 2900, Dallas, Texas 75201.

II. JURISDICTION AND VENUE

14. This action arises under the patent laws of the United States, Title 35 of the United Stated Code. The Court's jurisdiction over this action is proper under the above statutes, including 35 U.S.C. § 271 *et seq.*, and 28 U.S.C. §§ 1331 and 1338(a).

15. Personal jurisdiction exists generally over, Spansion, Intel, Numonyx, STMicro, Nokia, Sony Ericsson, and Motorola because they have sufficient minimum contacts with the forum as a result of business regularly conducted within the State of Texas and within the Northern District of Texas. Personal jurisdiction also exists specifically over the Defendants as a result of, at least, the Defendants' distribution network wherein the Defendants place their infringing products within the stream of commerce, which stream is directed at this district, and by committing the tort of patent infringement within the Northern District of Texas.

16. Venue is proper in this Court under 28 U.S.C. §§ 1391 (b), (c), and (d), as well as 28 U.S.C. § 1400(b).

III. PATENT INFRINGEMENT

17. Fast Erase repeats and re-alleges the allegations in Paragraphs 1 through 16 as though fully set forth herein.

18. Fast Erase is the owner of all rights, title and interest in and under United States Patent No. 6,236,608 ("the '608 Patent"), which duly and legally issued on May 22, 2001. The '608 Patent is for an invention titled "Technique To Improve The Source Leakage Of Flash EPROM Cells During Source Erase." A true and correct copy of the '608 patent is attached hereto as Exhibit A.

19. Fast Erase is the owner of all rights, title and interest in and under United States Patent No. 6,303,959 ("the '959 Patent"), which duly and legally issued on October 16, 2001. The '959 Patent is for an invention titled "Semiconductor Device Having Reduced Source Leakage During Source Erase." A true and correct copy of the '959 patent is attached hereto as Exhibit B.

20. The '608 Patent is valid and enforceable.

21. The '959 Patent is valid and enforceable.

22. Fast Erase has complied with the requirements of 35 U.S.C. § 287.

23. Upon information and belief, Spansion has been and is infringing, literally and/or under the doctrine of equivalents, the '608 Patent by making, using, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of one or more claims of the '608 Patent, including, but not limited to, NOR Flash products utilizing floating gate technologies.

24. By making, using, selling, offering for sale, and/or importing into the United States, without authority, products that fall within the scope of the claims of the '608 Patent, Spansion has also induced infringement of the '608 Patent under 35 U.S.C. § 271(b), and has

contributed to the infringement of the '608 Patent under 35 U.S.C. § 271(c). The infringing products have no substantial non-infringing uses.

25. Upon information and belief, STMicro has been and is infringing literally and/or under the doctrine of equivalents, the '608 Patent by making, using, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of one or more of the claims of the '608 Patent, including, but not limited to, NOR Flash products utilizing floating gate technologies.

26. By making, using, selling, offering for sale, and/or importing into the United States, without authority, products that fall within the scope of the claims of the '608 Patent, STMicro has also induced infringement of the '608 Patent under 35 U.S.C. § 271(b), and has contributed to the infringement of the '608 Patent under 35 U.S.C. § 271(c). The infringing products have no substantial non-infringing uses.

27. Upon information and belief, Numonyx has been and is infringing literally and/or under the doctrine of equivalents, the '608 Patent by making, using, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of one or more of the claims of the '608 Patent, including, but not limited to, NOR Flash products utilizing floating gate technologies.

28. By making, using, selling, offering for sale, and/or importing into the United States, without authority, products that fall within the scope of the claims of the '608 Patent, Numonyx has also induced infringement of the '608 Patent under 35 U.S.C. § 271(b), and has contributed to the infringement of the '608 Patent under 35 U.S.C. § 271(c). The infringing products have no substantial non-infringing uses.

29. Upon information and belief, Nokia has been and is infringing literally and/or

under the doctrine of equivalents, the '608 Patent by making, using, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of one or more of the claims of the '608 Patent, including, but not limited to, cellular handsets including NOR Flash products that utilize floating gate technologies.

30. By making, using, selling, offering for sale, and/or importing into the United States, without authority, products that fall within the scope of the claims of the '608 Patent, Nokia has also induced infringement of the '608 Patent under 35 U.S.C. § 271(b), and has contributed to the infringement of the '608 Patent under 35 U.S.C. § 271(c). The infringing products have no substantial non-infringing uses.

31. Upon information and belief, Motorola has been and is infringing literally and/or under the doctrine of equivalents, the '608 Patent by making, using, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of one or more of the claims of the '608 Patent, including, but not limited to, cellular handsets including NOR Flash products that utilize floating gate technologies.

32. By making, using, selling, offering for sale, and/or importing into the United States, without authority, products that fall within the scope of the claims of the '608 Patent, Motorola has also induced infringement of the '608 Patent under 35 U.S.C. § 271(b), and has contributed to the infringement of the '608 Patent under 35 U.S.C. § 271(c). The infringing products have no substantial non-infringing uses.

33. Upon information and belief, Intel has been and is infringing literally and/or under the doctrine of equivalents, the '959 Patent by making, using, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of one or more of the claims of the '959 Patent, including, but not limited to, Intel Strataflash NOR

Flash products.

34. By making, using, selling, offering for sale, and/or importing into the United States, without authority, products that fall within the scope of the claims of the '959 Patent, Intel has also induced infringement of the '959 Patent under 35 U.S.C. § 271(b), and has contributed to the infringement of the '959 Patent under 35 U.S.C. § 271(c). The infringing products have no substantial non-infringing uses.

35. Upon information and belief, Numonyx has been and is infringing literally and/or under the doctrine of equivalents, the '959 Patent by making, using, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of one or more of the claims of the '959 Patent, including, but not limited to, Strataflash NOR Flash products.

36. By making, using, selling, offering for sale, and/or importing into the United States, without authority, products that fall within the scope of the claims of the '959 Patent, Numonyx has also induced infringement of the '959 Patent under 35 U.S.C. § 271(b), and has contributed to the infringement of the '959 Patent under 35 U.S.C. § 271(c). The infringing products have no substantial non-infringing uses.

37. Upon information and belief, Sony Ericsson has been and is infringing literally and/or under the doctrine of equivalents, the '959 Patent by making, using, offering for sale, and/or importing in or into the United States, without authority, products that fall within the scope of one or more of the claims of the '959 Patent, including, but not limited to, cellular handsets including Strataflash NOR Flash products.

38. By making, using, selling, offering for sale, and/or importing into the United States, without authority, products that fall within the scope of the claims of the '959 Patent,

Sony Ericsson has also induced infringement of the '959 Patent under 35 U.S.C. § 271(b), and has contributed to the infringement of the '959 Patent under 35 U.S.C. § 271(c). The infringing products have no substantial non-infringing uses.

39. Upon information and belief, Spansion, Intel, STMicro, Numonyx, Nokia, Sony Ericsson, and Motorola had knowledge of the '608 and '959 Patents but have engaged in their infringing conduct nonetheless. Spansion's, Intel's, STMicro's, Numonyx's, Nokia's, Sony Ericsson's, and Motorola's infringement is therefore willful.

40. Fast Erase has no adequate remedy at law against these acts of patent infringement. Unless Spansion, Intel, ST Micro, Numonyx, Nokia, Sony Ericsson, and Motorola are permanently enjoined from its unlawful and willful infringement of the '608 or '959 Patents, Fast Erase will suffer irreparable harm.

41. As a direct and proximate result of Spansion's, Intel's, STMicro's, Numonyx's, Nokia's, Sony Ericsson's, and Motorola acts of patent infringement, Fast Erase, has been and continues to be injured and has sustained and will continue to sustain substantial damages in an amount not presently known.

42. Fast Erase has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute create an exceptional case within the meaning of 35 U.S.C. § 285, and Fast Erase is entitled to recover its reasonable and necessary fees and expenses.

IV. PRAYER FOR RELIEF

Fast Erase requests that judgment be entered in its favor and against Spansion, Intel, STMicro, Numonyx, Nokia, Sony Ericsson, and Motorola and that the Court grant the following relief to Fast Erase:

(a) Declare that the '608 and '959 Patent are valid and enforceable;

(b) Declare that Spansion, Intel, STMicro, Numonyx, Nokia, Sony Ericsson, and Motorola have infringed the '608 and '959 Patents;

(c) Declare that Spansion's, Intel's, STMicro's, Numonyx's, Nokia's, Sony Ericsson's, and Motorola's infringement was willful;

(d) Award damages to Fast Erase to which it is entitled for patent infringement of the '608 and '959 Patents;

(e) Enter a preliminary, and thereafter, permanent injunction against Spansion, Intel, STMicro, Numonyx, Nokia, Sony Ericsson, and Motorola for direct infringement of the '608 and '959 Patents;

(f) Enter a preliminary, and thereafter, permanent injunction against Spansion, Intel, STMicro, Numonyx, Nokia, Sony Ericsson and Motorola for active inducement of infringement and/or contributory infringement of the '608 and '959 Patents by others;

(g) Award Fast Erase its expenses, costs, and attorneys fees pursuant to 35 U.S.C. § 285;

(h) Award Fast Erase increased damages in an amount not less than (3) three times the amount of damages found by the jury or assessed by this Court for Spansion's, Intel's, ST Micro's,Numonyx's, Nokia's, Sony Ericsson's, and Motorola's willful infringement pursuant to 35 U.S.C. § 284;

(i) Award interest on Fast Erase's damages; and

(j) Such other relief as the Court deems just and proper.

V. JURY DEMAND

In accordance with Federal Rules of Civil Procedure 38 and 39, Fast Erase asserts its rights under the Seventh Amendment of the United States Constitution and demands a trial by jury on all issues.

Dated: June 9, 2008

Respectfully submitted,

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Attorneys for Plaintiff
Fast Memory Erase, LLC

EXHIBIT A

US006236608B1

(12) **United States Patent**
Ratnam

(10) **Patent No.: US 6,236,608 B1**
(45) **Date of Patent: May 22, 2001**

(54) **TECHNIQUE TO IMPROVE THE SOURCE LEAKAGE OF FLASH EPROM CELLS DURING SOURCE ERASE**

(75) Inventor: **Perumal Ratnam**, Fremont, CA (US)

(73) Assignee: **Alliance Semiconductor**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/375,702**

(22) Filed: **Aug. 16, 1999**

(51) **Int. Cl.**[7] **G11C 13/00**
(52) **U.S. Cl.** **365/218**; 365/226
(58) **Field of Search** 365/218, 185.33, 365/185.29, 226

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,120,671		6/1992	Tang et al.	437/43
5,470,773		11/1995	Liu et al.	437/43
5,791,204	*	11/1999	Haaa	365/218
6,005,809	*	12/1999	Sung et al.	365/218

OTHER PUBLICATIONS

Chang, et al., "Corner–Field Induced Drain Leakage In Thin Oxide MOSFETs," *IEDM Technical Digest*, 31.2,pp. 714–717 (1987).

Kume,et al., "A Flash–Erase EEPROM Cell With an Asymmetric Source and Drain Structure," *IEDM Technical Digest*25.8, pp. 560–563 (1987).

Yokozawa, et al., "Low–Field–Stress Erasing Scheme for Highly–Reliable Flash Memories," NEC ULSI Device Development Laboratories, 24 pages, Feb. 12, 1997.

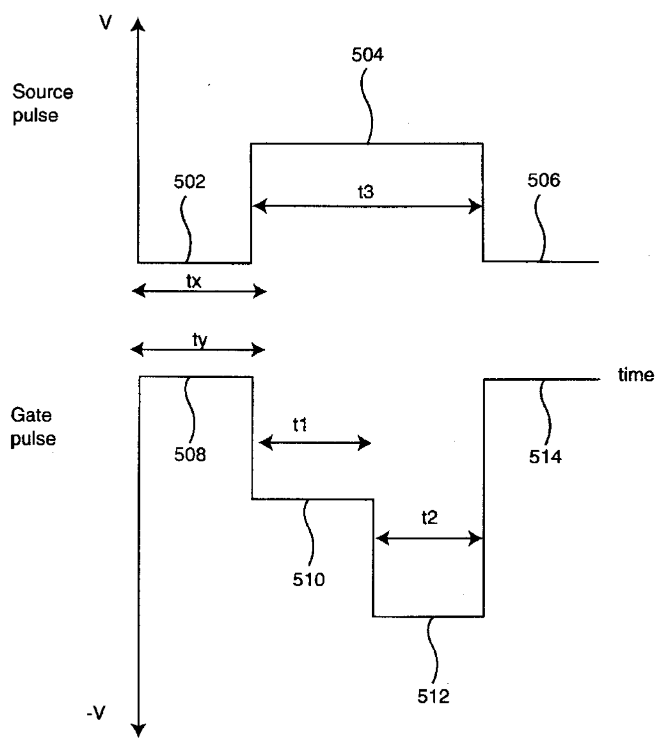
* cited by examiner

Primary Examiner—Terrell W. Fears
(74) *Attorney, Agent, or Firm*—Beyer Weaver & Thomas, LLP

(57) **ABSTRACT**

In one aspect, the present invention provides a method for erasing a semiconductor device that comprises applying a voltage pulse at the source of the semiconductor device and a multiple step voltage pulse of the opposite polarity at the gate of the semiconductor device. The multiple step voltage pulse comprises at least a first voltage pulse and a second voltage pulse at the gate of the semiconductor device. The second voltage pulse is usually greater in magnitude than the first voltage pulse. In another aspect, the present invention provides a method for erasing a semiconductor device that comprises applying a substantially constant positive voltage pulse for a first time interval, t_1, at the source of the semiconductor device. A first and then a second negative voltage pulse are also applied at the gate of the semiconductor device for a second and third time interval, t_2 and t_3, respectively. The second negative voltage pulse is greater in magnitude than the first negative voltage pulse. The negative and positive voltage pulses are substantially coincident in time.

28 Claims, 10 Drawing Sheets



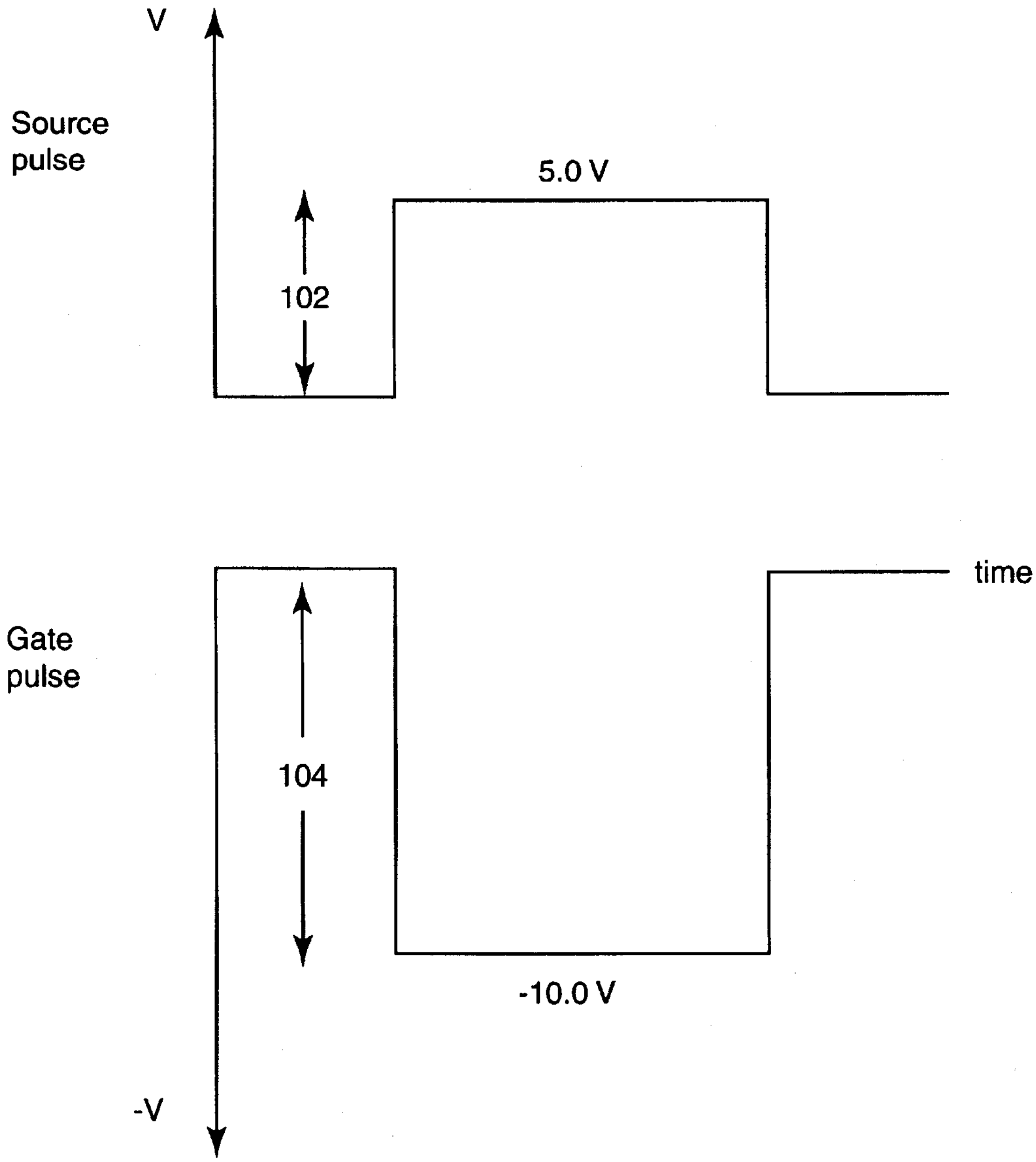


Figure 1
Prior Art

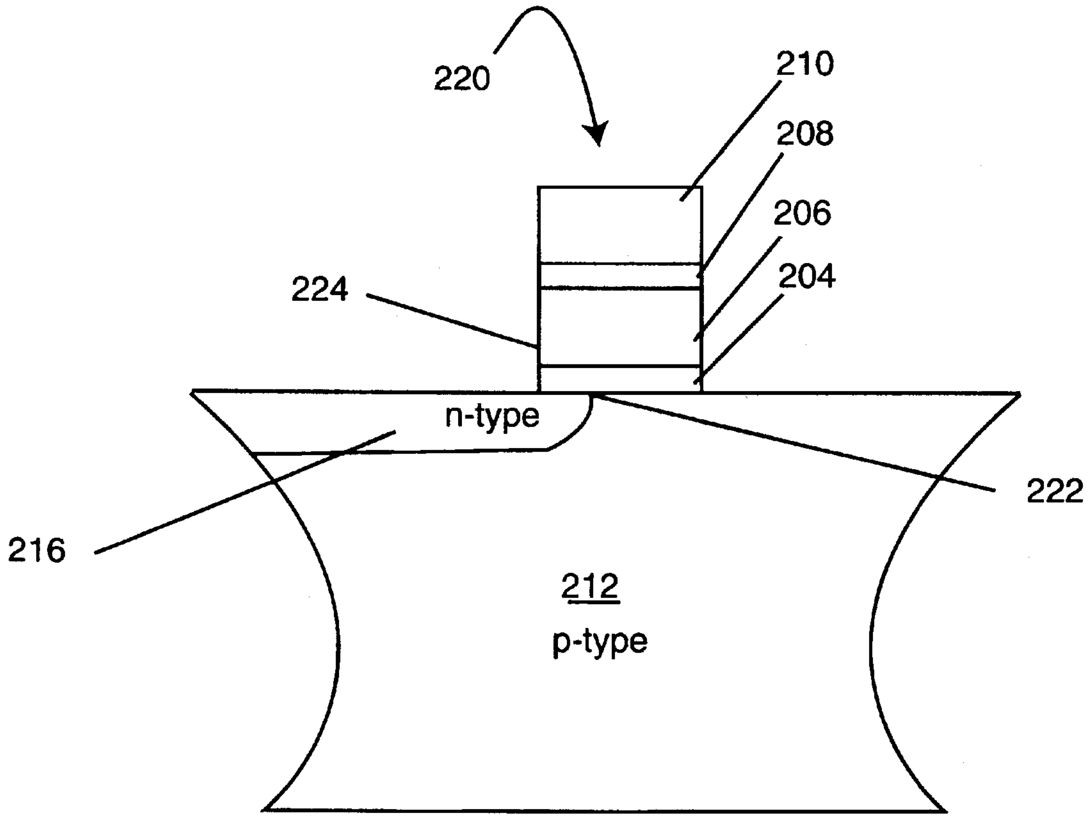


Figure 2
PRIOR ART

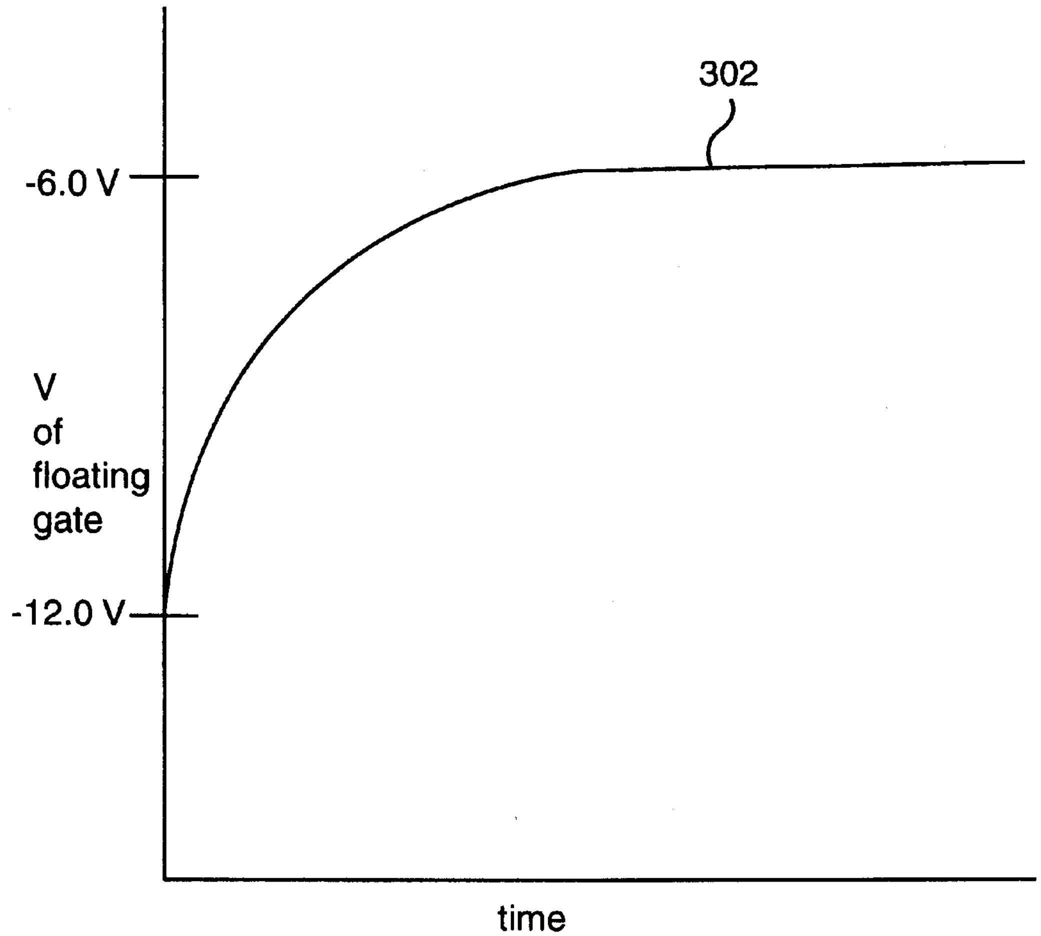


Figure 3
PRIOR ART

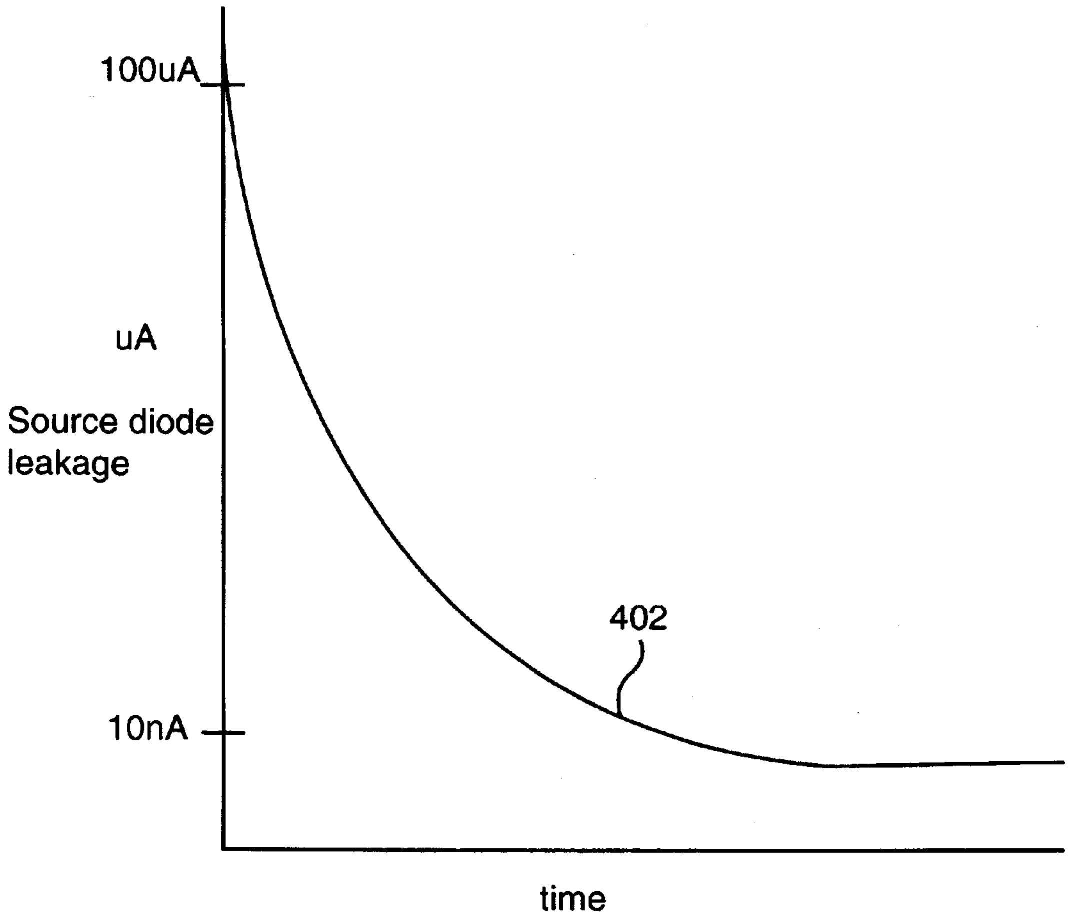


Figure 4
PRIOR ART

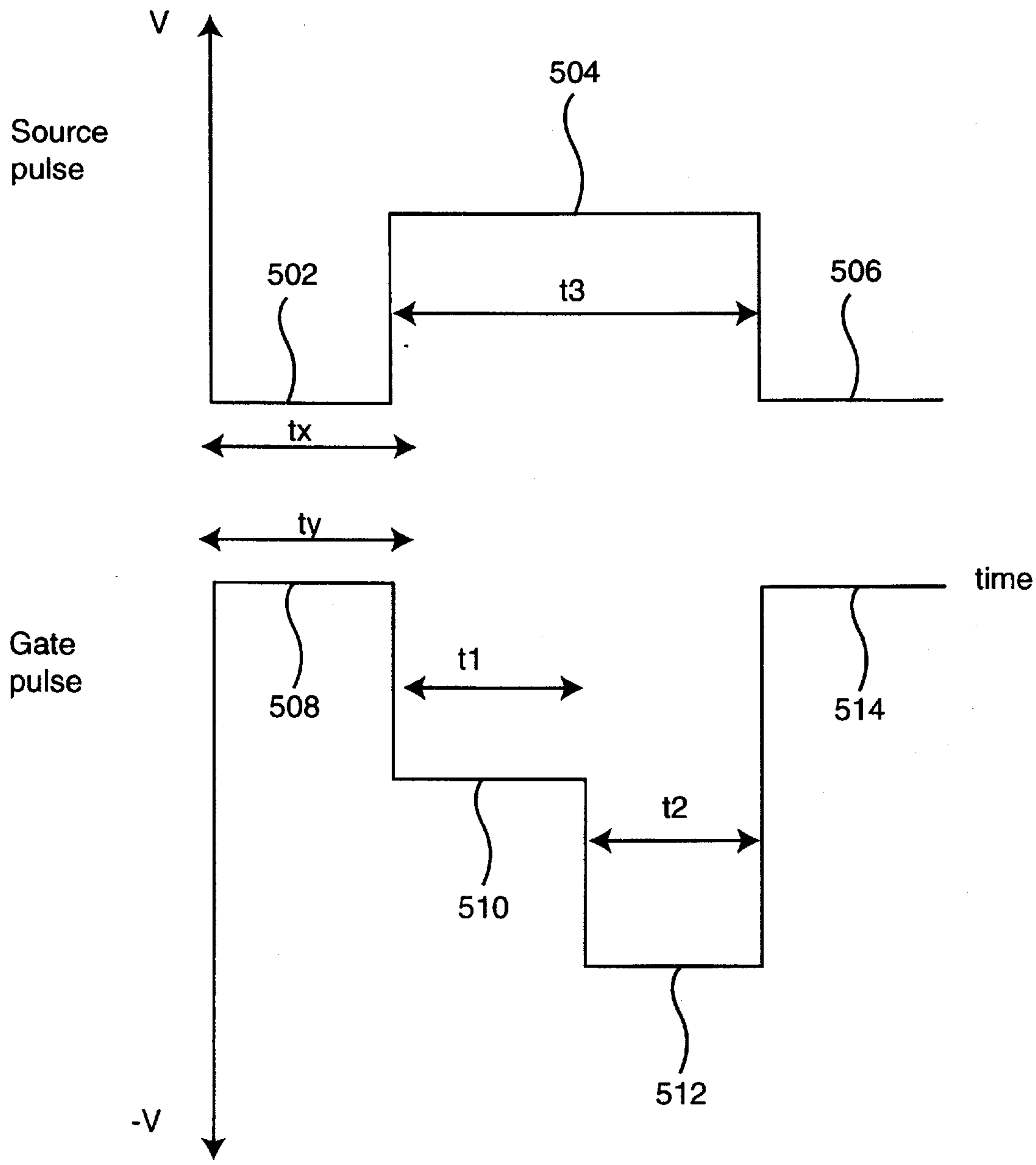

V
504
Source
pulse
502
t3
506
tx
ty
time
Gate
pulse
t1
508
514
t2
510
512
-V

Figure 5

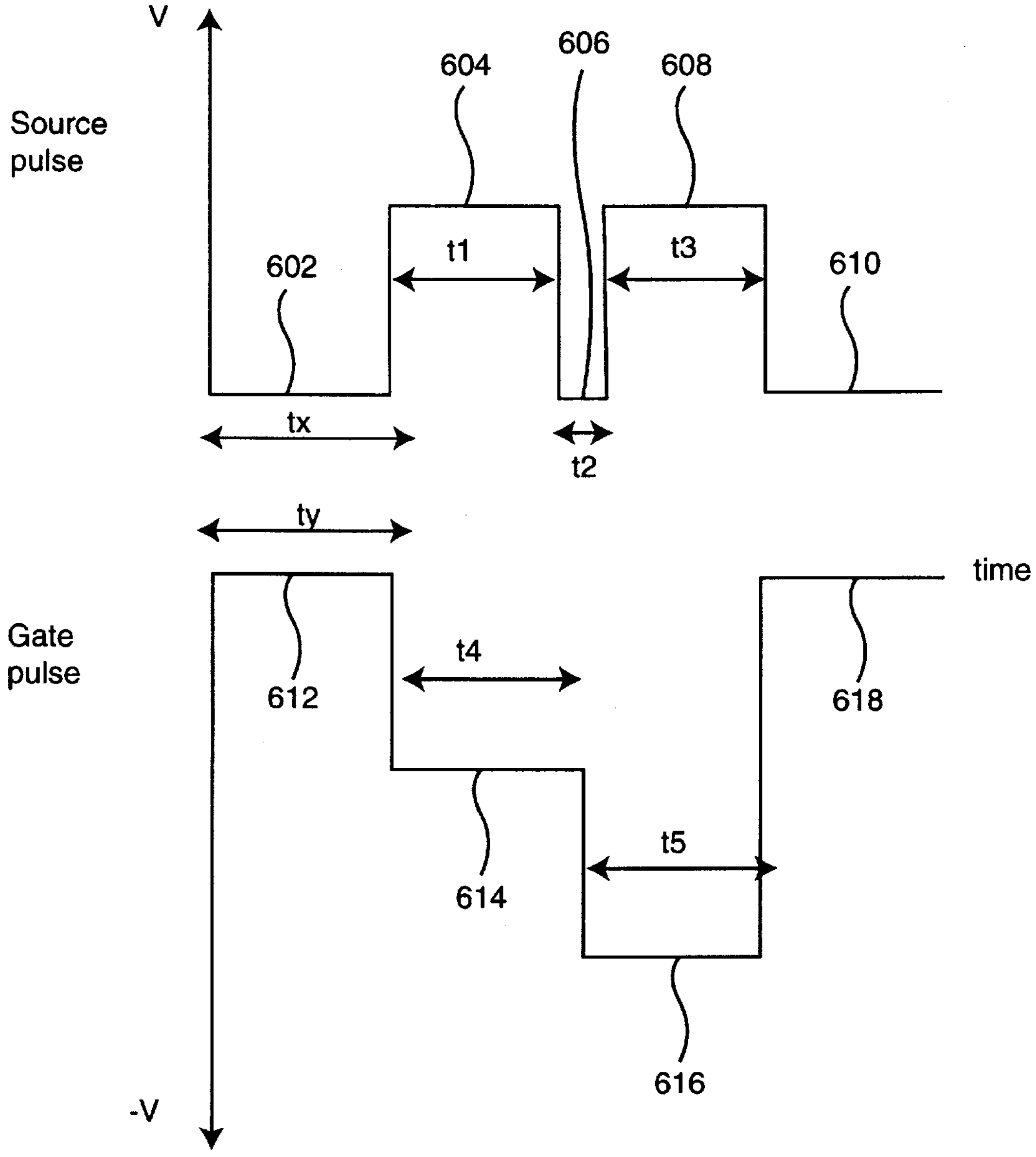

V
Source
pulse
602
604
606
608
610
t1
t3
tx
t2
ty
time
Gate
pulse
612
t4
618
614
t5
616
-V

Figure 6

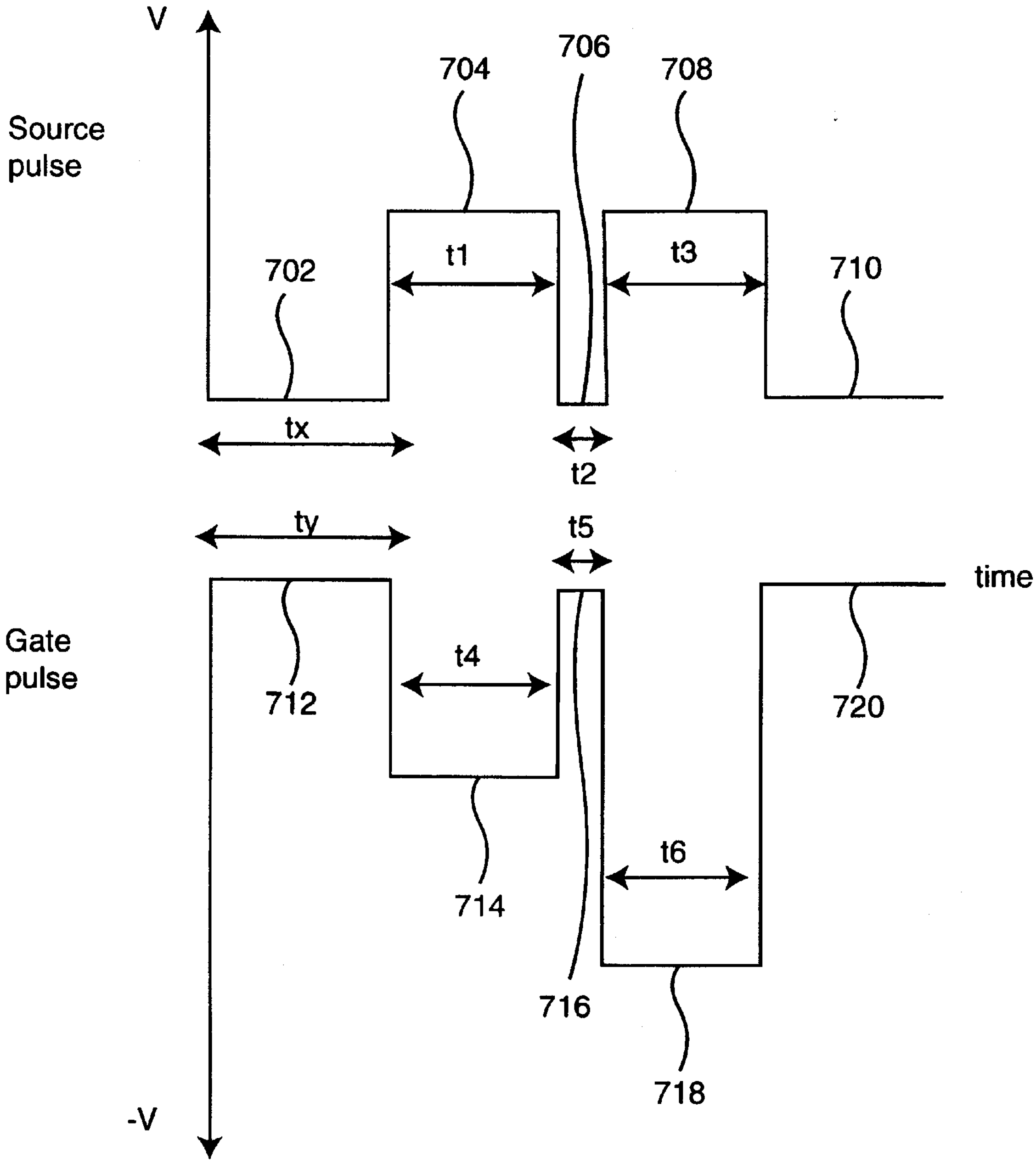

V
704
706
708
Source
pulse
t1
t3
702
710
tx
t2
ty
t5
time
Gate
pulse
t4
712
720
t6
714
716
718
-V

Figure 7

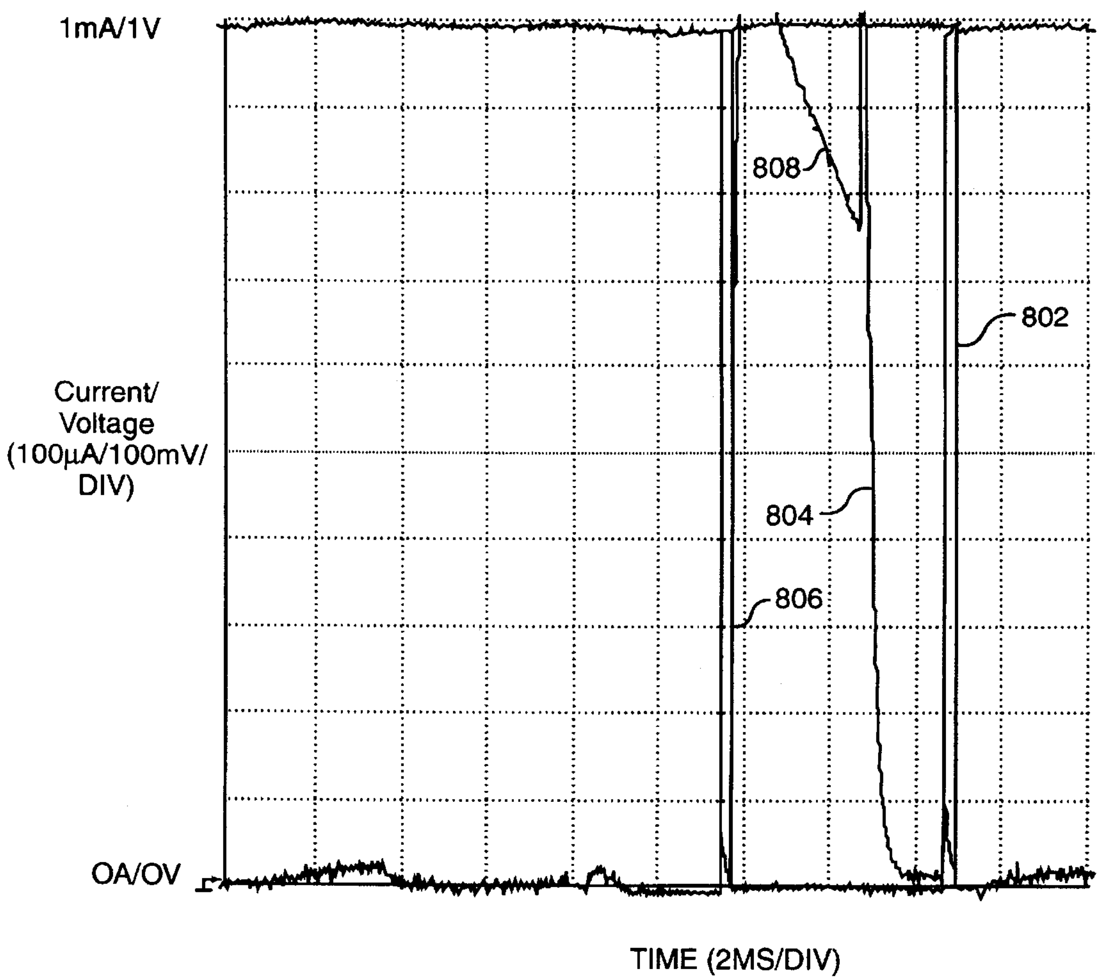

1mA/1V
Current/
Voltage
(100µA/100mV/
DIV)
OA/OV
808
802
804
806
TIME (2MS/DIV)

Figure 8A

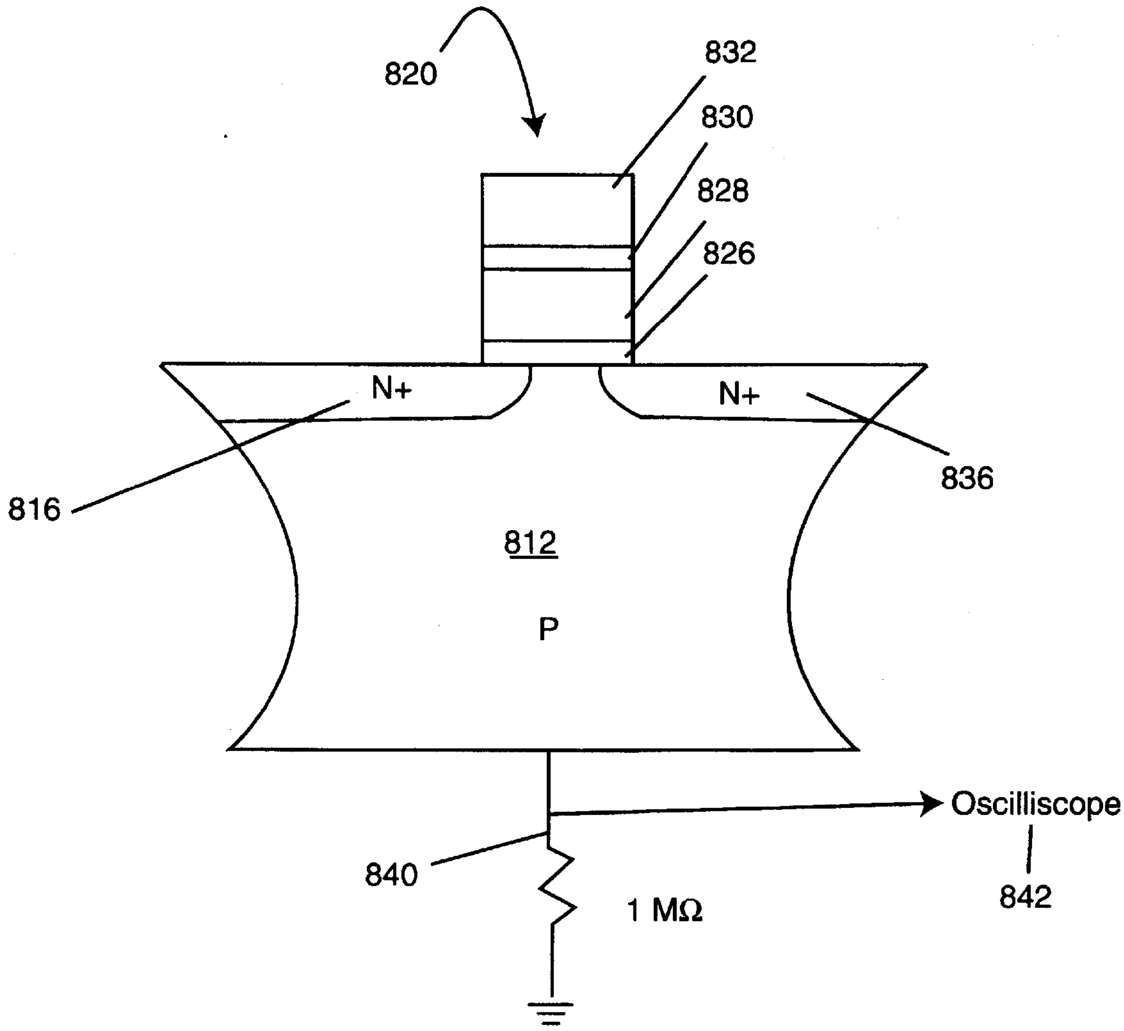
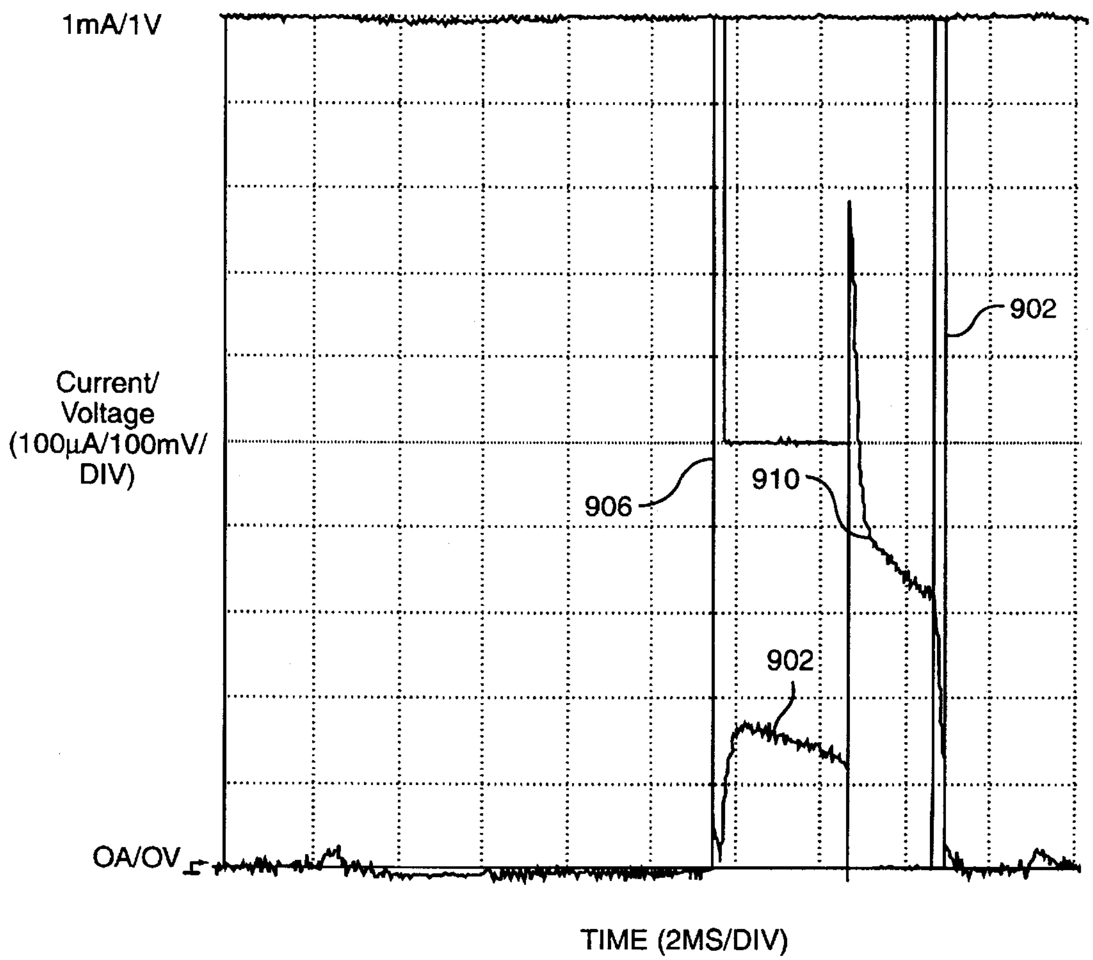


Figure 8B



1mA/1V
Current/
Voltage
(100µA/100mV/
DIV)
OA/OV
902
906
910
902
TIME (2MS/DIV)

Figure 9

TECHNIQUE TO IMPROVE THE SOURCE LEAKAGE OF FLASH EPROM CELLS DURING SOURCE ERASE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to flash EPROM cells and methods for their construction. More particularly, the current invention relates to reducing leakage during source erase of a flash EPROM cell. More specifically, the present invention provides a new erase technique that reduces leakage during source erase of a flash EPROM cell.

2. Discussion of Related Art

Erasable programmable read-only memory (EPROM) is a form of non-volatile memory. Non-volatile memory devices retain information when power to the device is interrupted and are important in the design of wireless and portable electronic devices. Non-volatile storage choices range from mask read-only memory (ROM), ultraviolet EPROM (UV-EPROM), flash EPROM and electrically erasable EPROM (EEPROM).

EPROM devices typically lack the density of ROM disks but are more flexible since coded changes can be readily accommodated. EPROM devices offer the further advantage of rapid access since reading and writing to these types of devices is not delayed by latency periods.

Flash EPROM offers some of the advantages of EEPROM with the lower cost of UV-EPROM. All forms of EPROM use electrical injection methods to program individual memory cells but differ in the method of memory cell erasure. Ultraviolet light irradiation is used to erase UV-EPROM memory cells. This method is non-selective and requires removal of memory cells from the system for erasure. EEPROM systems use Fowler-Nordheim tunneling to erase single cells which offers reprogramming flexibility, high density and convenience, since removal of memory cells from the device is not required for erasure.

Flash EPROM also uses Fowler-Nordheim tunneling for non-selective memory cell erasure. Thus, flash EPROM provides the convenience and high density of EEPROM with the low cost of conventional UV-EPROM. Therefore, flash EPROM has become the storage method of choice in many portable consumer devices such as cell phones and hand held personal computers.

Two different methods, which employ Fowler-Nordheim tunneling, are typically used to erase flash EPROM cells. In channel or substrate erase, a positive bias of about 10.0 V is applied to the substrate of the memory cell. Similarly, a negative bias of about −5.0 V is applied to the gate of the memory cell. Electron tunneling from the gate to the substrate then erases the memory cell. Channel erase requires source isolation by the triple well process, which is complicated and expensive.

Source erase is identical to substrate erase except that a positive bias of about 5.0 V is applied to the source of the memory cell while a negative bias of about −10.0 V is applied to the gate of the memory cell. Since source erase does not require source isolation by the triple well process it is simpler and less expensive to implement than channel erase.

However, a significant problem with source erase of flash EPROM cells is source diode leakage to the substrate during erasure. Source diode leakage lengthens the time required to erase a flash EPROM, degrades performance and must be minimized to increase source erase speed.

Three different mechanisms have been identified as contributing to source diode leakage during source erase. Thermal leakage, which is intrinsic to any tunneling process, is small and independent of electric field. Avalanche multiplication is electric field dependent and can become very large if the cell is not optimized during fabrication.

Band to band tunneling leakage is a fundamental problem with source erase, particularly at high electrical field and reduced channel width (C. Chang et al., *Tech. Dig. IEDM,* 714, 1987; H. Kume et al., *Tech. Dig. IEDM,* 560, 1987). Band to band tunneling leakage wastes power since some of the diode current is dissipated in the substrate during erasure. Furthermore, constant source voltage is difficult to maintain in the presence of this type of leakage, which places significant demand on the charge pump capacitor. Thus, the difficulties caused by band to band leakage in generating and maintaining the voltage required to erase the device are frequently the limiting factor in erasure of flash EPROM cells.

FIG. **1** illustrates a conventional method used to erase a flash EPROM cell. Shown in FIG. **1** are conventional source and gate pulse profiles as a function of time. The source pulse height **102** is about 5.0 V while the gate pulse height **104** is about −10.0 V during memory cell erasure. The gate pulse height **102** and source pulse height **104** strongly affect the erase speed and are typically adjusted to maximize electron tunneling from the floating gate to the source. However, optimizing erasure rate increases the magnitude of the source to gate electric field, thus causing significant band to band tunneling leakage.

The relationship of conventional erase techniques and band to band tunneling leakage may be understood with reference to FIGS. **2**, **3** and **4**. Shown in FIG. **2** is a stacked gate **220** disposed on a semiconductor substrate **212**. The stacked gate **220** may be made by conventional methods well known in the art. Stacked gate **220** is comprised of tunnel oxide layer **204**, a floating gate **206**, insulating layer **208** and the control gate **210**. Floating gate **206** and control gate **210** are typically different polysilicon layers. Source **216** forms an electrical junction with the stacked gate **220** at the source edge **222** under the stacked gate edge **224**.

Typically, in a programmed cell a residual electric field of about −2.0 V to about −3.0 V exists between the source **216** and the stacked gate **220**. Thus, applying a voltage of between about −10.0 V and about −12.0 V to the control gate **210** instantaneously results in an effective voltage of between about −12.0 V to about −15.0 V in floating gate **206**. Therefore, a high electric field exists in the floating gate **206** upon initial voltage application until some of the electrons tunnel to source **216**. The voltage in the floating gate eventually reaches a constant value as excess electrons tunnel to the source.

The dependence of floating gate voltage on time after initial voltage application to the control gate is graphically depicted in FIG. **3**. The vertical axis represents the voltage of the floating gate while the horizontal axis represents time. Line **302** in FIG. **3** reaches a constant value as a function of time. The electric field in the floating gate changes from an initial value of about −12.0 V to a constant value of about −6.0 V within about 100 μsec. Thus, the electric field in the floating is diminished by a factor of about 2 during about 100 μsec. The change in voltage reflects tunneling of electrons to the source.

However, as previously mentioned, the high initial electric field in the floating gate results in a large source diode current due to band to band tunneling leakage. FIG. **4**

graphically illustrates the relationship between source diode leakage caused by band to band tunneling as a function of time after initial application of voltage to the control gate. The horizontal axis represents the amount of leakage to the substrate from the source diode caused by band to band tunneling while the horizontal axis represents time. Line **402** rapidly decays from an initial value of about 100 μA to a constant value of about 10 nA in about 100 μsec. Thus, the amount of current leaked into the source is diminished by a factor of about ten in 100 μsec. As can be seen from FIG. **4** a significant percentage of source diode leakage occurs after initial application of voltage to the control gate.

FIGS. **3** and **4** demonstrate that a significant problem in source erase is the high initial electric field in the floating gate, which consequently results in high initial source diode leakage. As electrons are removed from the floating gate source diode leakage is also reduced.

It has become apparent that as flash EPROM devices shrink in size and increase in density that new methods of reducing source diode leakage are necessary. Thus, what is needed is a new erase technique that minimizes band to band tunneling leakage during source erase. More particularly, what is required is a method that reduces the magnitude of source diode leakage caused by high initial electric field in the floating gate

SUMMARY OF THE INVENTION

The present invention addresses this need by providing a new method that reduces initial source diode leakage by varying the gate pulse height during source erase while the source pulse height is held substantially constant. Importantly, the method of the present invention reduces source diode leakage caused by high initial electric field in the floating gate.

The method of the current invention provides a first voltage pulse of low magnitude to the gate of the semiconductor device, which reduces the initial electric field in the floating gate in comparison to prior art methods. Consequently, source diode leakage to the substrate is significantly diminished. Then, after the voltage of the floating gate has declined to a substantially constant value, a second voltage pulse of high magnitude is applied to the gate of the semiconductor device. Thus, the method of the present invention offers the advantage of rapid source erase with a high magnitude voltage pulse and low source diode leakage. Furthermore, the method of the current invention is most useful in modern semiconductor devices of decreasing channel length where the capacity of source charge pumps is particularly limited.

In one aspect, the present invention provides a method for erasing a semiconductor device that includes applying a voltage pulse at the source of the semiconductor device and a multiple step voltage pulse of the opposite polarity at the gate of the semiconductor device. The multiple step voltage pulse includes at least a first voltage pulse and a second voltage pulse at the gate of the semiconductor device. The second voltage pulse is greater in magnitude than the first voltage pulse.

In a first embodiment, the multiple step voltage pulse applied at the gate includes applying the first voltage pulse for a first time interval, t_1, and the second voltage pulse for a second time interval, t_2. The voltage pulse at the source of the semiconductor device is applied for a third time interval, t_3. In this embodiment, a voltage pulse applied at the source of the semiconductor device is substantially constant, and the multiple step voltage pulse at the gate and the voltage

pulse at the source are substantially coincidental in time ($t_1+t_2=t_3$). Note that this is not a required condition as t_1+t_2 may also be greater than or less than t_3.

In a second embodiment, the voltage pulse applied at the source of the semiconductor device includes applying a first voltage pulse for a first time interval, t_1, and a substantially identical second voltage pulse for a third time interval, t_3. A second time interval, t_2, where the voltage applied to the source is about zero separates t_1 and t_3. The multistep voltage pulse applied at the gate of the semiconductor device is substantially coincidental with $t_1+t_2+t_3$. In this embodiment, the multiple step voltage pulse includes applying a third voltage pulse for a fourth time interval, t_4, and a fourth higher voltage pulse for a fifth time interval, t_5, where $t_1+t_2+t_3=t_4+t_5$. Note that this is not a required condition as $t_1+t_2+t_3$ may also be greater or less than t_4+t_5.

In a third embodiment, the voltage pulse applied at the source of the semiconductor device includes applying a first voltage pulse for a first time interval, t_1, and a substantially identical second voltage pulse for a third time interval, t_3. A second time interval, t_2, where the voltage applied to the source is about zero separates t_1 and t_3. In this embodiment, the multiple step voltage pulse includes applying a third voltage pulse for a fourth time interval, t_4, and a fourth higher voltage pulse for a sixth time interval, t_6. A fifth time interval, t_5, the voltage applied to the gate is about zero separates t_4 and t_6. In this embodiment, $t_1+t_2+t_3=t_4+t_5+t_6$. Note that this is not a required condition as $t_1+t_2+t_3$ may also be greater than or less than $t_4+t_5+t_6$. The multiple step voltage pulse and the voltage pulse are substantially coincidental in time.

In another aspect, the present invention provides a method for erasing a semiconductor device that includes applying a substantially constant positive voltage pulse for a first time interval, t_1, at the source of the semiconductor device. A first and then a second negative voltage pulse are also applied at the gate of the semiconductor device for a second and third time interval, t_2 and t_3, respectively. The second negative voltage pulse is greater in magnitude than the first negative voltage pulse. The negative and positive voltage pulses are substantially coincidental in time.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the following description taken in conjunction with the accompanying drawings in which:

FIG. **1** illustrates conventional source and gate pulse profiles as a function of time;

FIG. **2** illustrates a conventional stacked gate on a semiconductor substrate;

FIG. **3** illustrates the dependence of floating gate voltage on time;

FIG. **4** illustrates the dependence of source diode leakage on time;

FIG. **5** illustrates source and gate pulse profiles as a function of time for a first embodiment of the present invention;

FIG. **6** illustrates source and gate pulse profiles as a function of time for a second embodiment of the present invention;

FIG. **7** illustrates source and gate pulse profiles as a function of time for a third embodiment of the present invention;

FIG. **8A** illustrates a digitizing oscilloscope scan of source erasure for a prior art method;

FIG. 8B illustrates source leakage measurement with a resistor at the substrate terminal; and

FIG. 9 illustrates a digitizing oscilloscope scan of source erasure using the method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the invention. Examples of preferred embodiments are illustrated in the accompanying drawings. While the invention will be described in conjunction with preferred embodiments, it will be understood that it is not intended to limit the invention to these preferred embodiments. To the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

The present invention provides a method that reduces initial source diode leakage by changing the gate pulse height during source erase while holding the source pulse height substantially constant. The method of the present invention reduces source diode leakage caused by high initial electric field in the floating gate.

In a first embodiment, the present invention provides a method for erasing a semiconductor device that employs a multistep gate voltage pulse to minimize source diode leakage. FIG. **5** illustrates the source and gate pulse profiles of one embodiment of the current invention as a function of time.

Initially, the voltage **502** applied to the source of the semiconductor device is about zero. After a period of time represented by t_x a voltage pulse **504** is applied to the source of a semiconductor device as shown in FIG. **5**. The voltage pulse **504** may be equivalent to the maximum allowable source pulse height. In one embodiment, the voltage pulse **504** is between about 4.0 V and about 5.0 V. In a more specific embodiment, the voltage pulse **504** is about 4.5 V.

Voltage pulse **504** may be applied for a time interval, represented by t_3 in FIG. **5**. In one embodiment, t_3 is between about 100 μsec and about 100 msec. In a more specific embodiment, t_3 is about 500 μsec. Voltage pulse **504** is substantially constant during time interval t_3. After time interval t_3 has elapsed, the voltage **506** applied to the source of the semiconductor device drops to about zero.

The initial voltage **508** applied to the gate of the semiconductor device is about zero. After a period of time represented by t_y, voltage pulse **510** is applied to the gate of the semiconductor device as shown in FIG. **5**. The period of time t_y may larger, smaller or equal to the period of time t_x. Generally, voltage pulse **510** will be less than the maximum allowable gate pulse height. In one embodiment, voltage pulse **510** is between about −4.0 V and about −6.0 V. In a more specific embodiment, voltage pulse **510** is about −5.0 V.

Voltage pulse **510** may be applied for a time interval represented by t_1 in FIG. **5**. In one embodiment, t_1 is between about 250 μsec and about 500 μsec. In a more specific embodiment, t_1 is about 300 μsec. Voltage pulse **510** is substantially constant during time interval t_1.

After time interval t_1 has elapsed, voltage pulse **512** may be applied to the gate of the semiconductor device. Generally, voltage pulse **512** will be about the maximum allowable gate pulse height. Usually, voltage pulse **512** will be greater in magnitude than voltage pulse **510**. In one embodiment, the voltage pulse is between about −9.0 V and about −11.0 V. In a more specific embodiment, voltage pulse **512** is about −10.0 V.

Voltage pulse **512** may be applied for a time interval, represented by t_2 in FIG. **5**. In one embodiment, t_2 is between about 100 μsec and about 300 μsec. In a more specific embodiment, t_2 is about 200 μsec. Voltage pulse **510** is substantially constant during time interval t_2. After time interval t_2 has elapsed, the voltage **514** applied to the gate of the semiconductor device drops to about zero.

The source and gate voltage pulses will usually be applied at about the same time during source erasure, although this is not an essential condition. The time intervals for the source and gate voltage pulses may be about the same ($t_1+t_2=t_3$). Note that this is not a required condition as t_1+t_2 may also be greater than or less than t_3. In the exemplified embodiment, $t_1=t_2$ which also is not a required condition since t_1 may also be greater or less than t_2.

Importantly, the gate voltage pulse sequence may be applied in more than two steps. For example, the gate voltage pulse may be varied in a sequence comprising 0.0 V to −2.0 V to −5.0 V to −7.0 V to −10.0 V. Alternatively, the gate voltage may be steadily decreased from about 0.0 V to about −10.0 V without distinct steps, like a ramp voltage.

FIG. **6** illustrates the source and gate pulse profiles as a function of time for a second embodiment of the current invention. In this embodiment, the source pulse profile has been altered to reduce system noise due to switching of levels, which are derived from charge pumps.

Referring now to FIG. **6**, the voltage **602** initially applied to the source of the semiconductor device is about zero. Voltage pulse **604** is then applied to the source of a semiconductor device after a period of time represented by t_x as shown in FIG. **6**. Voltage pulse **604** may be the maximum allowable source pulse height. In one embodiment, voltage pulse **604** is between about 4.0 V and about 5.0 V. In a more specific embodiment, voltage pulse **604** is about 4.5 V.

Voltage pulse **604** may be applied for a time interval, which is represented by t_1 in FIG. **6**. In one embodiment, t_1 is between about 100 μsec and about 300 μsec. In a more specific embodiment, t_1 is about 200 μsec. Voltage pulse **604** is substantially constant for time interval t_1.

After time interval t_1 has elapsed, the voltage **606** applied to the source of the semiconductor device is reduced to about zero for a time interval represented by t_2 in FIG. **6**. As explained before, voltage break **606** reduces system noise. Generally, t_2 is much smaller than t_1. In one embodiment, t_2 is between about 10 μsec and about 30 μsec. In a more specific embodiment, t_2 interval is about 20 μsec.

After time interval t_2 has elapsed, voltage pulse **608** is applied to the source of a semiconductor device as shown in FIG. **6**. Voltage pulse **608** may be equivalent to the maximum allowable source pulse height. Usually, voltage pulse **608** is substantially identical to voltage pulse **604**. In one embodiment, voltage pulse **608** is between about 4.0 V and about 5.0 V. In a more specific embodiment, voltage pulse **608** is about 4.5 V.

Voltage pulse **608** may be applied for a time interval represented by t_3 in FIG. **6**. In one embodiment, t_3 is between about 100 μsec and about 300 μsec. In a more specific embodiment, t_3 is about 200 μsec. Voltage pulse **608** is substantially constant during time interval t_3. After time interval t_3 has elapsed, the voltage **610** applied to the gate of the semiconductor device drops to about zero.

The initial voltage **612** applied to the gate of the semiconductor device is about zero. After a period of time

represented by t_y, voltage pulse **614** is applied to the gate of the semiconductor device as shown in FIG. **6**. The period of time t_y may larger, smaller or equal to the period of time t_x. Usually, voltage pulse **614** will be less than the maximum allowable gate pulse height. In one embodiment, voltage pulse **614** is between about −4.0 V and about −6.0 V. In a more specific embodiment, voltage pulse **614** is about −5.0 V.

Voltage pulse **614** may be applied for a time interval represented by t_4 in FIG. **6**. In one embodiment, t_4 is between about 100 μsec and about 300 μsec. In a more specific embodiment, t_4 is about 210 μsec. Voltage pulse **614** is substantially constant during time interval t_4.

After time interval t_4 has elapsed, voltage pulse **616** may be applied to the gate of the semiconductor device. Generally, voltage pulse **616** will be about the maximum allowable gate pulse height. Usually, voltage pulse **616** is greater in magnitude than voltage pulse **614**. In one embodiment, voltage pulse **616** is between about −9.0 V and about −11.0 V. In a more specific embodiment, voltage pulse **616** is about −10.0 V.

Voltage pulse **616** may be applied for a time interval, represented by t_5 in FIG. **6**. In one embodiment, t_5 is between about 100 μsec and about 300 μsec. In a more specific embodiment, t_5 is about 210 μsec. Voltage pulse **616** is substantially constant during time interval t_5. After time interval t_5 has elapsed, the voltage **618** applied to the gate of the semiconductor device is reduced to about zero.

The source and gate voltage pulses will usually be applied at about the same time during source erasure, although this is not an essential condition. The time intervals for the source and gate voltage pulses may be about the same ($t_1+t_2+t_3=t_4+t_5$). Note that this is not a required condition as $t_1+t_2+t_3$ may also be greater or less than t_4+t_5. In the exemplified embodiment, $t_1=t_3$ and $t_4=t_5$ which also are not required conditions since t_1 may also be greater or less than t_2 and t_4 may also be greater or less than t_5.

FIG. **7** illustrates the source and gate pulse profiles as a function of time for a third embodiment of the current invention. In this embodiment, both the source and gate pulse profiles have been altered to reduce system noise.

Referring now to FIG. **7**, the voltage **702** initially applied to the source of the semiconductor device is about zero. Voltage pulse **704** is then applied to the source of a semiconductor device after a period of time represented by t_x as shown in FIG. **7**. Voltage pulse **704** may be the maximum allowable source pulse height. In one embodiment, voltage pulse **704** is between about 4.0 V and about 6.0 V. In a more specific embodiment, voltage pulse **704** is about 5.0 V.

Voltage pulse **704** may be applied for a time interval, which is represented by t_1 in FIG. **7**. In one embodiment, t_1 is between about 100 μsec and about 300 μsec. In a more specific embodiment, t_1 is about 200 μsec. Voltage pulse **704** is substantially constant for time interval t_1.

After time interval t_1 has elapsed, the voltage **706** applied to the source of the semiconductor device is reduced to about zero for a time interval represented by t_2 in FIG. **7**. Generally, t_2 is much smaller than t_1. In one embodiment, t_2 is between about 10 μsec and about 30 μsec. In a more specific embodiment, t_2 interval is about 20 μsec.

After time interval t_2 has elapsed, voltage pulse **708** is applied to the source of a semiconductor device as shown in FIG. **6**. Voltage pulse **708** may be equivalent to the maximum allowable source pulse height. Usually, voltage pulse **708** is substantially identical to voltage pulse **704**. In one embodiment, voltage pulse **708** is between about 4.0 V and about 6.0 V. In a more specific embodiment, voltage pulse **708** is about 5.0 V.

Voltage pulse **708** may be applied for a time interval represented by t_3 in FIG. **6**. In one embodiment, t_3 is between about 100 μsec and about 300 μsec. In a more specific embodiment, t_3 is about 200 μsec. Voltage pulse **708** is substantially constant during time interval t_3. After time interval t_3 has elapsed, the voltage **710** applied to the source of the semiconductor device is reduced to about zero.

The voltage **712** initially applied to the gate of the semiconductor device is about zero. After a period of time represented by t_y voltage pulse **714** is applied to the gate of a semiconductor device as shown in FIG. **7**. The period of time t_y may larger, smaller or equal to the period of time t_x. In one embodiment, voltage pulse **714** is between about −4.0 V and about −6.0 V. In a more specific embodiment, the first voltage pulse **714** is about −5.0 V.

Voltage pulse **714** may be applied for a time interval represented by t_4 in FIG. **7**. In one embodiment, t_4 is between about 100 μsec and about 300 μsec. In a more specific embodiment, t_4 is about 200 μsec. Voltage pulse **714** is substantially constant during time interval t_4.

After t_4 has elapsed, the voltage **716** applied to the gate of the semiconductor device is reduced to about zero for a time interval represented by t_5 in FIG. **7**. Voltage break **716**, as explained before, causes system noise reduction. Usually, t_5 is much smaller than t_4. In one embodiment, time interval t_5 is between about 10 μsec and about 30 μsec. In a more specific embodiment, time interval t_5 is about 20 μsec.

After time interval t_5 has elapsed, voltage pulse **718** is applied to the gate of a semiconductor device as shown in FIG. **7**. Usually, voltage pulse **718** is greater than voltage pulse **714**. In one embodiment, voltage pulse **718** is between about −9.0 V and about −11.0 V. In a more specific embodiment, voltage pulse **718** is about −10.0 V.

Voltage pulse **718** may be applied for a time interval represented by t_6 in FIG. **7**. In one embodiment, t_6 is between about 100 μsec and about 300 μsec. In a more specific embodiment, t_6 is about 200 μsec. Voltage pulse **718** is substantially constant during time interval t_6. After time interval t_6 has elapsed, the voltage **720** applied to the gate of the semiconductor device is reduced to about zero.

The source and gate voltage pulses will usually be applied at about the same time during source erasure although this is not an essential condition. The time intervals for the source and gate voltage pulses may be about the same ($t_1+t_2+t_3=t_4+t_5+t_6$). Note that this is not a required condition as $t_1+t_2+t_3$ may also be greater or less than $t_4+t_5+t_6$. In the exemplified embodiment, $t_1=t_3$, $t_2=t_5$ and $t_4=t_6$ which also are not required conditions since t_1 may also be greater or less than t_3, t_2 may also be greater or less than t_5 and t_4 may also be greater or less than t_6.

EXAMPLE

The following example describes specific aspects of the invention to illustrate the invention and also provide a description of the experimental conditions to aid those of skill in the art in understanding and practicing the invention. The example should not be construed as limiting the invention in any manner.

FIG. **8A** illustrates a digitizing oscilloscope scan using a prior art method for source erasure. The vertical axis represents source leakage current while the horizontal axis represents time.

The source leakage current is measured with a resistor at the substrate terminal as illustrated in FIG. **8B**. Shown in

FIG. **8**B is a stacked gate **820** disposed on a semiconductor substrate **812**. The stacked gate **820** may be made by conventional methods well known in the art. Stacked gate **820** is comprised of tunnel oxide layer **826**, a floating gate **828**, oxide layer **830** and the control gate **832**. Floating gate **828** and control gate **832** are typically different polysilicon layers. Source **816** and drain **834** are partially disposed under the stacked gate **820**. A source pulse is applied at source **816** and a gate pulse is applied at stacked gate **820**. The source leakage is measure by resistor **840** attached to the substrate terminal as shown which is connected to oscilloscope **842**.

Referring now to FIG. **8**A, the resistance of the substrate used in this example was about 1 MΩ. Here, the voltage pulse **802** applied at the source is about 5.0 V for a time interval of 5.5 msec and is offscale since the scale of the vertical axis of the scan is from 0–1 V which is equal 0–1 μA. The gate is pulsed first at about −10.0 V for about 3.0 msec at **804** and at about −10.0 V at **806** for about 2.0 msec. Thus, the applied voltage at both the source and the gate is constant. The average leakage **808** is about 900 nA.

FIG. **9** illustrates a digitizing oscilloscope scan using the method of the current invention for source erasure. The vertical axis represents voltage and current while the horizontal axis represents time. The resistance of the substrate used in this example was about 1 MΩ. Here, the voltage pulse **902** at the source is again about 5.0 V for a time interval of 5.5 msec and is offscale. The gate is pulsed first at about −5.0 V for about 3.0 msec and at about −10 V for about 2.0 msec at **906**. The leakage is about 150 nA for the first pulse at **908** and about 350 nA at **910** for the second pulse.

This above example shows the efficacy of the method of the present invention in reducing source diode leakage during source erasure.

The described embodiments of the present invention offer significant advantages over the prior art. FIG. **4** demonstrated that a significant amount of source diode leakage occurred immediately following initial application of voltage to the control gate. The method of the current invention provides a first voltage pulse of low magnitude to the gate of the semiconductor device, which reduces the initial electric field in the floating gate in comparison to prior art methods. Consequently, source diode leakage to the substrate is significantly diminished. Then, after the voltage of the floating gate has declined to a substantially constant value, a second voltage pulse of high magnitude is applied to the gate of the semiconductor device. Thus, the method of the present invention offers the advantage of rapid source erase with a high magnitude voltage pulse and low source diode leakage. Furthermore, the method of the current invention is most useful in modern semiconductor devices of decreasing channel length where the capacity of source charge pumps is particularly limited.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims.

Furthermore, it should be noted that there are alternative ways of implementing the process of the present invention. For example, the gate pulse profile illustrated in FIG. **7** could be combined with the source profile illustrated in FIG. **5**. Different time intervals and voltages could be used to implement the current invention. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

1. A method for erasing a semiconductor device comprising:

applying a voltage pulse at the source of the semiconductor device; and

applying a multiple step voltage pulse of the opposite polarity, said multiple step voltage pulse having at least a first voltage pulse and a second voltage pulse, at the gate of the semiconductor device;

wherein said second voltage pulse is greater in magnitude than said first voltage pulse.

2. The method of claim **1**, wherein the multiple step voltage pulse comprises:

applying the first voltage pulse for a first time interval; and

applying the second voltage pulse for a second time interval;

wherein the first and second time intervals are substantially coincident with applying the voltage pulse at the source of the semiconductor device.

3. The method of claim **1**, wherein the voltage pulse at the source of the semiconductor device is between about 4.0 V and about 6.0 V.

4. The method of claim **1**, wherein the voltage pulse at the source of the semiconductor device is about 5.0 V.

5. The method of claim **1**, wherein the voltage pulse at the source of the semiconductor device comprises applying for a third time interval.

6. The method of claim **5**, wherein the third time interval is between about 100 μsec and about 100 msec.

7. The method of claim **5**, wherein the third time interval is about 500 μsec.

8. The method of claim **1**, wherein the first voltage pulse is between about −4.0 V and about −6.0 V.

9. The method of claim **1**, wherein the first voltage pulse is about −5.0 V.

10. The method of claim **1**, wherein the second voltage pulse is between about −9.0 V and about −11.0 V.

11. The method of claim **1**, wherein the second voltage pulse is about −10.0 V.

12. The method of claim **2**, wherein the first time interval is between about 250 μsec and about 500 μsec.

13. The method of claim **2**, wherein the first time interval is about 300 μsec.

14. The method of claim **2**, wherein the second time interval is between about 100 μsec and about 300 μsec.

15. The method of claim **2**, wherein the second time interval is about 200 μsec.

16. The method of claim **1**, wherein the voltage pulse at the source of the semiconductor device further comprises:

applying a third voltage pulse for a first time interval; and

applying a substantially identical fourth voltage pulse for a third time interval;

wherein the first time interval and the third time interval are separated by a second time interval during which no voltage is applied to the source of the semiconductor device.

17. The method of claim **16**, wherein the third voltage pulse and the fourth voltage pulse are about 5.0 V.

18. The method of claim **16**, wherein the first time interval is substantially identical to the third time interval.

19. The method of claim **16**, wherein the first time interval and the third time interval are greater than the second time interval.

20. The method of claim **16**, wherein the first time interval is between about 100 μsec and about 300 μsec, the second time interval is between about 10 μsec and about 30 μsec and the third time interval is between about 100 μsec and about 300 μsec.

21. The method of claim **16**, wherein the first time interval is about 200 μsec, the second time interval is about 20 μsec and the third time interval is about 200 μsec.

22. The method of claim **16**, wherein the multiple step voltage pulse at the gate of the semiconductor device comprises:

applying the first voltage pulse for a fourth time interval; and

applying the second voltage pulse for a sixth time interval;

wherein the first voltage pulse and the second voltage pulse are separated by a fifth time interval during which no voltage is applied to the gate of the semiconductor device.

23. The method of claim **22**, wherein the first voltage pulse is about −5.0 V and the second voltage pulse is about −10.0 V.

24. The method of claim **22**, wherein the fourth time interval is between about 100 μsec and about 300 μsec, the fifth time interval is between about 10 μsec and about 30 μsec and the sixth time interval is between about 100 μsec and about 300 μsec.

25. The method of claim **22**, wherein the fourth time interval is about 200 μsec, the fifth time interval is about 20 μsec and the sixth time interval is about 200 μsec.

26. A method for erasing a semiconductor device comprising:

applying a constant positive voltage pulse for a first time interval at the source of the semiconductor device;

applying a first negative voltage pulse for a second time interval at the gate of the semiconductor device; and

applying a second negative voltage pulse for a third time interval at the gate of the semiconductor device;

wherein said second negative voltage pulse is greater in magnitude than said first negative voltage pulse.

27. The method of claim **26**, wherein the constant positive voltage pulse is about 5.0 V.

28. The method of claim **26**, wherein the first negative voltage pulse is about −5.0 V and the second negative voltage pulse is about −10.0 V.

* * * * *

EXHIBIT B

US006303959B1

(12) **United States Patent**
Ratnam

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(54) **SEMICONDUCTOR DEVICE HAVING REDUCED SOURCE LEAKAGE DURING SOURCE ERASE**

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(52) **U.S. Cl.** **257/314**; 257/314; 257/315; 257/381; 257/637; 257/639; 438/954
(58) **Field of Search** 257/314, 315, 257/381, 385, 637, 639; 438/954

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Assistant Examiner—Edgardo Ortiz
(74) *Attorney, Agent, or Firm*—Beyer Weaver & Thomas, LLP

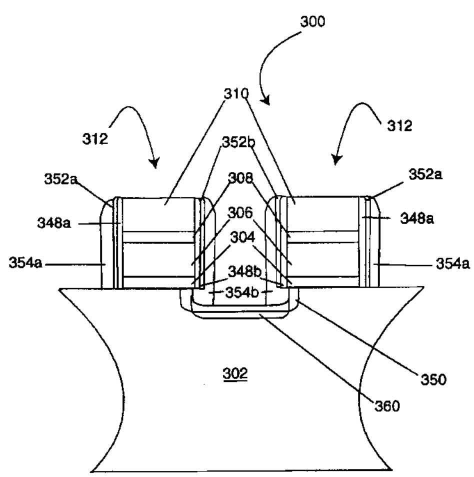
(57) **ABSTRACT**

In one aspect, the current invention provides a method for reducing the source leakage of a semiconductor device. The method comprises the steps of stacked gate etch, thin oxide formation, SAS etch, spacer formation and source implant on the semiconductor substrate.

In a second aspect, the current invention provides another method for reducing the source leakage of a semiconductor device. The method comprises the steps of stacked gate etch, first oxide layer formation, first source implant, annealing, SAS etch, second oxide layer formation, spacer formation, and second source implant.

In yet another aspect, the current invention provides a novel semiconductor device. The semiconductor device is comprised of a stacked gate provided on a portion of a semiconductor substrate, a first oxide layer appended to the stacked gate, a second oxide layer formed on the first oxide layer and a spacer formed on the second oxide layer. The semiconductor device also has a doped source region having a first doped region disposed under the edge of the stacked gate and a second doped region disposed at the edge of the doped source region under the stacked gate. The second doped region has a higher concentration of dopant than the first doped region, which reduces source leakage of the semiconductor device.

17 Claims, 15 Drawing Sheets



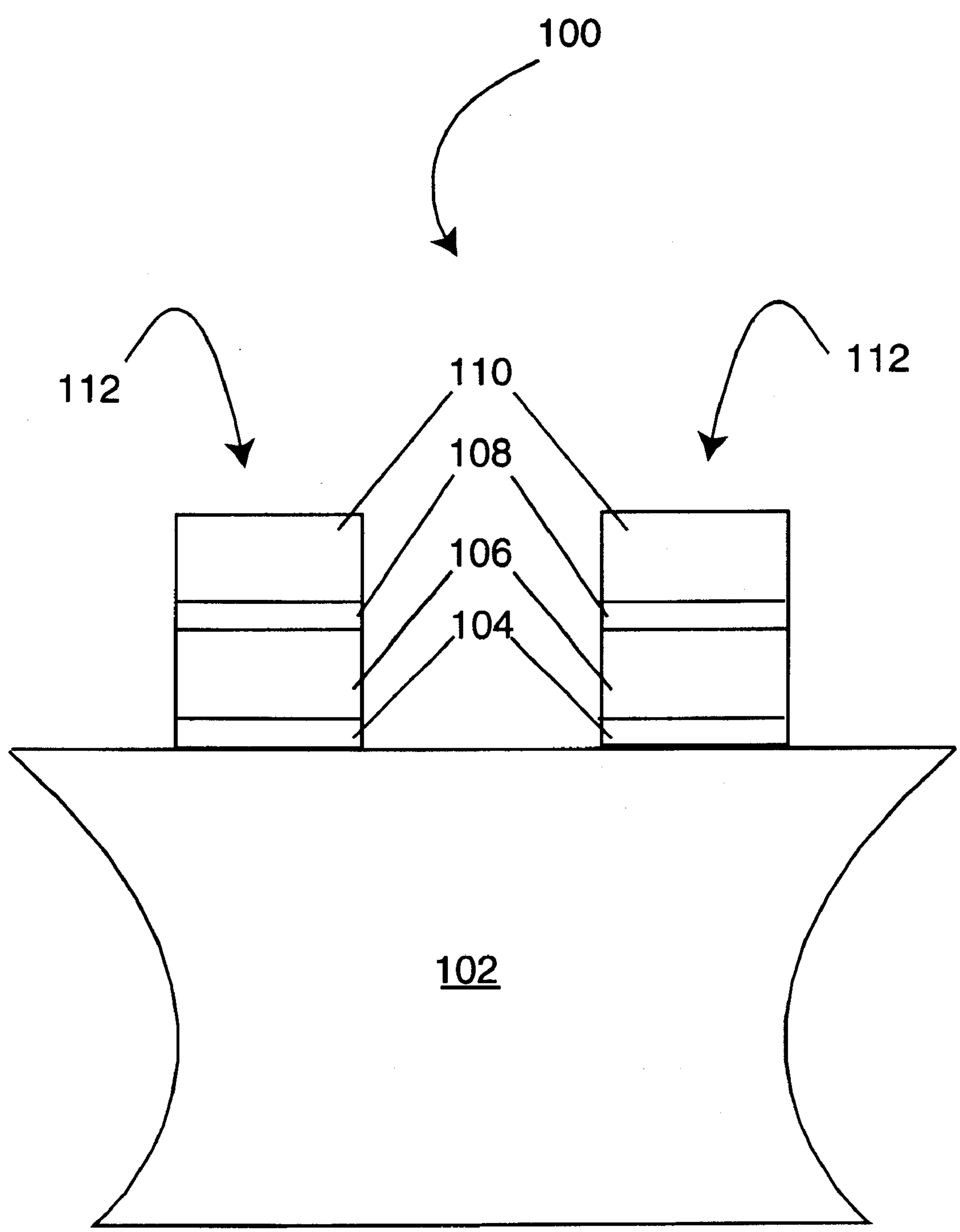


Figure 1

PRIOR ART

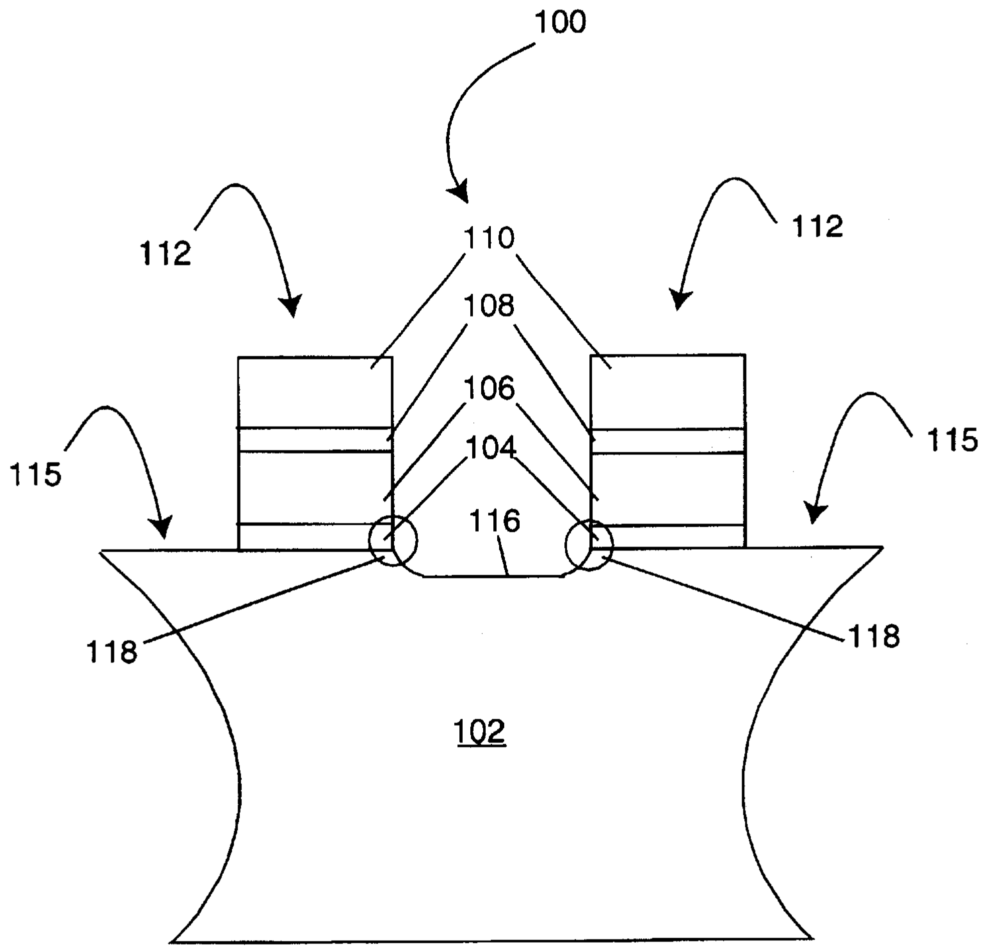


Figure 2A
PRIOR ART

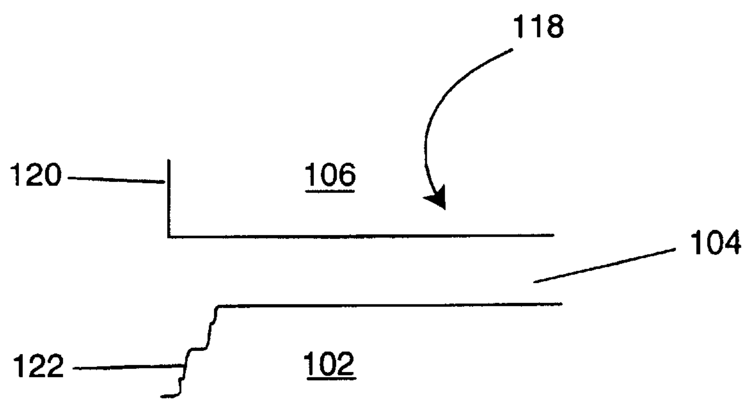


Figure 2B
PRIOR ART

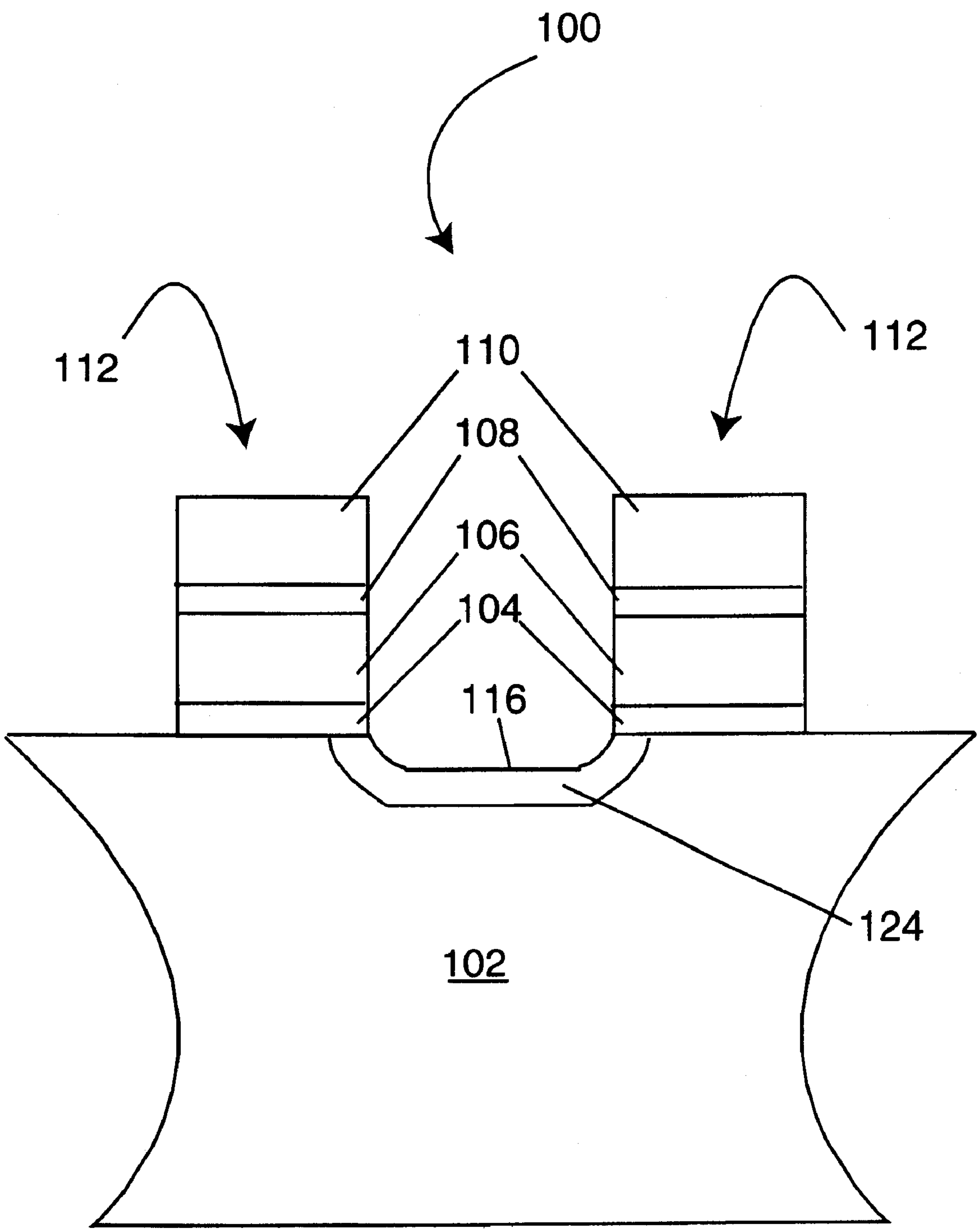


Figure 3

PRIOR ART

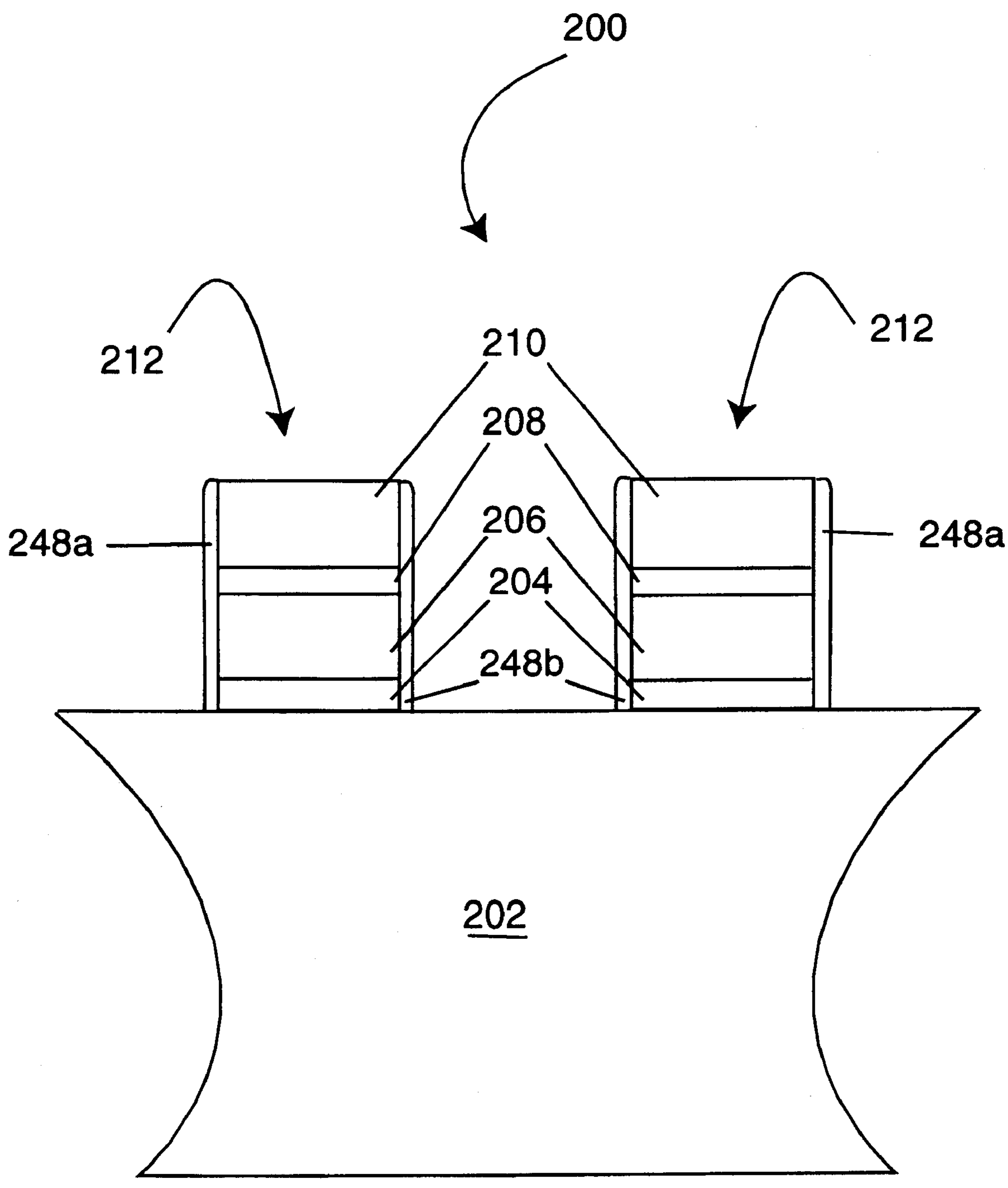


Figure 4

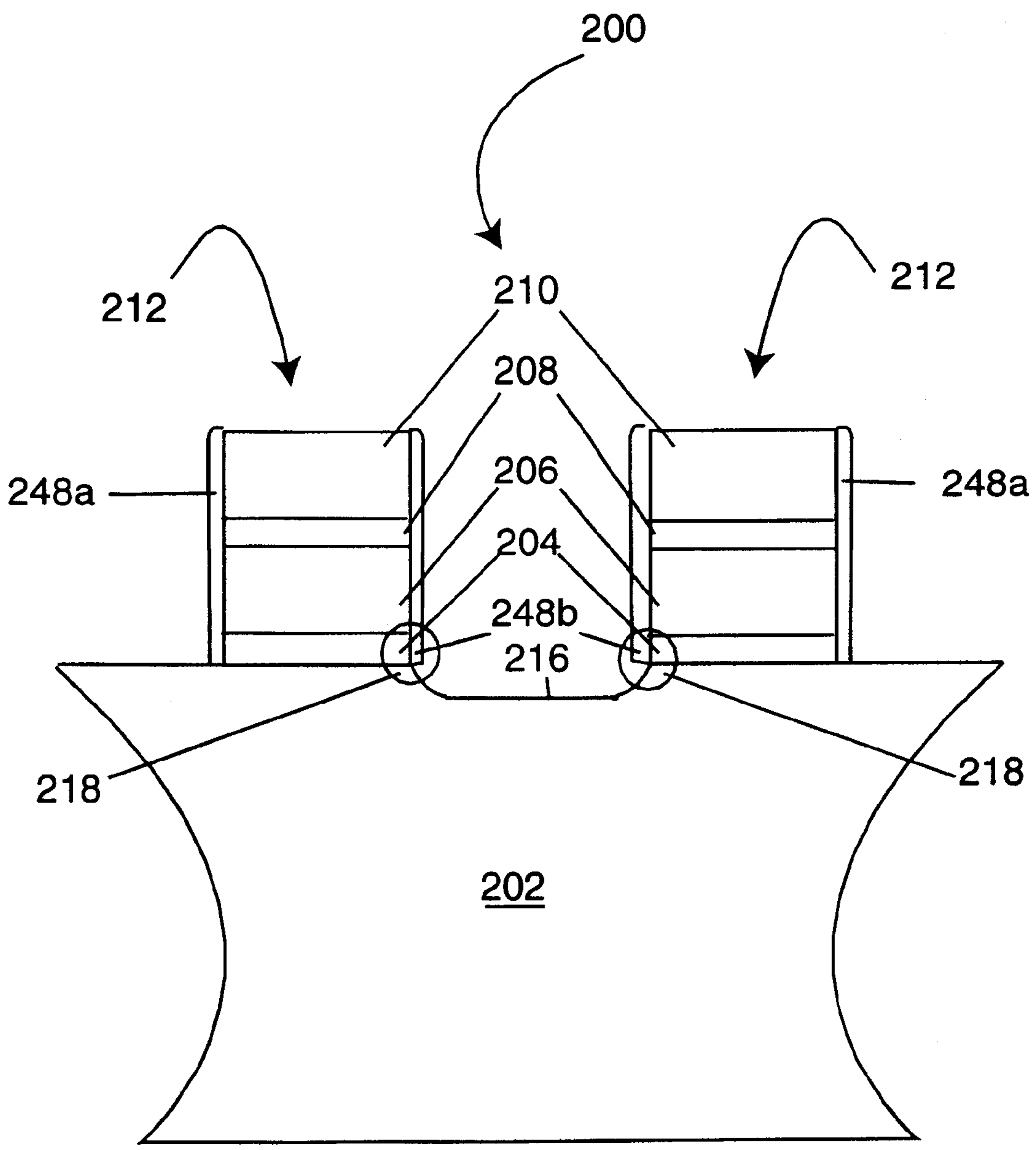


Figure 5

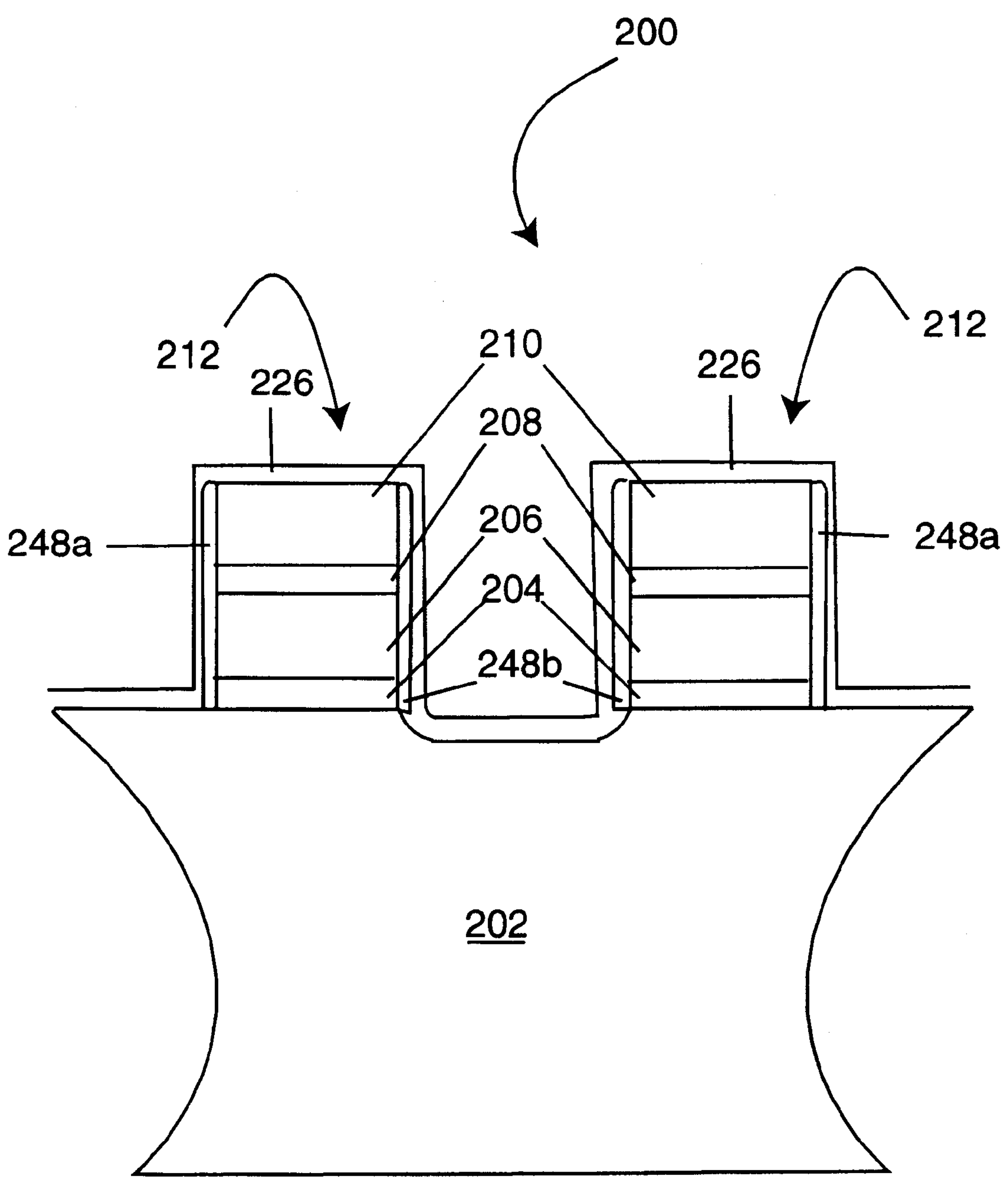


Figure 6

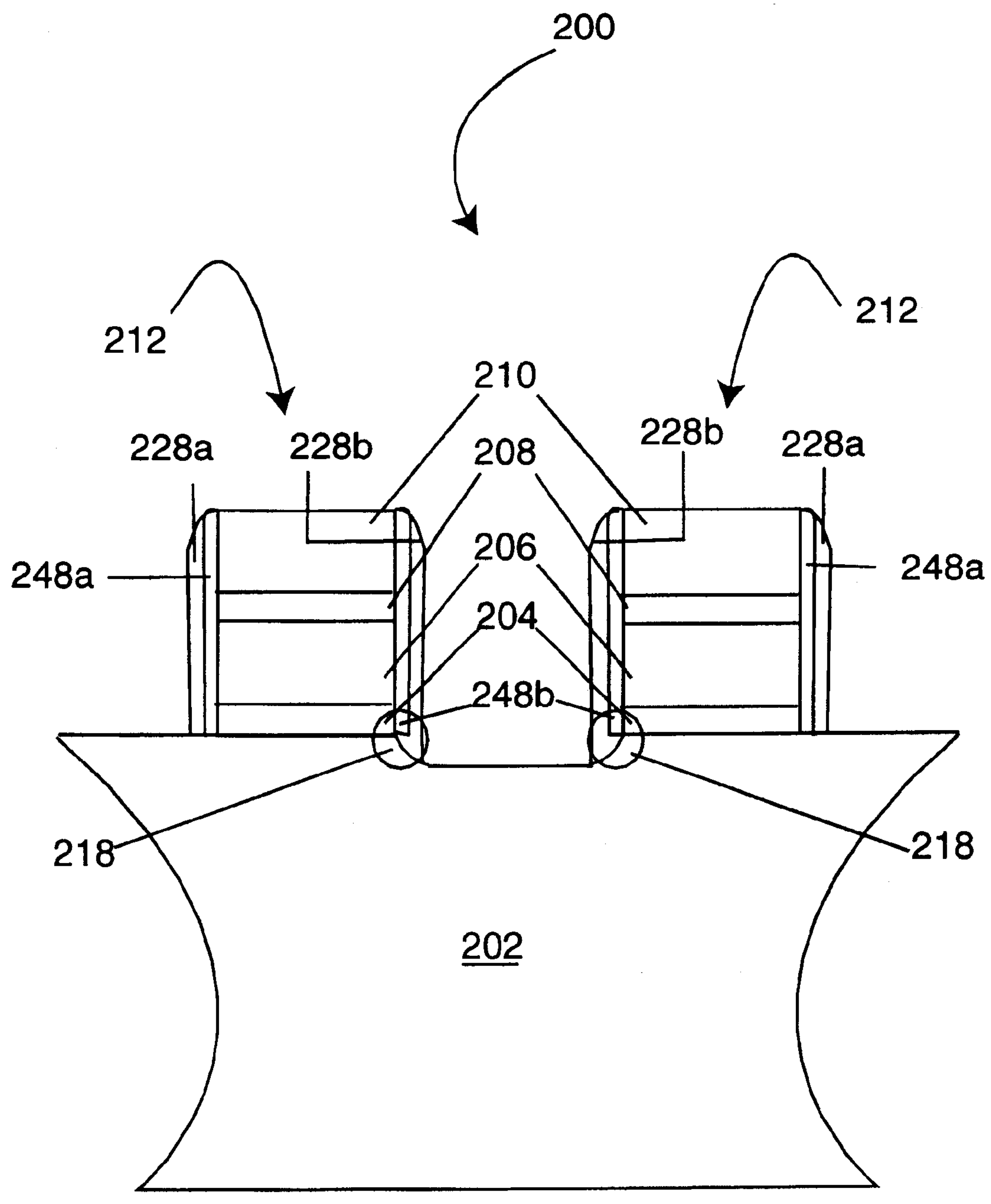

200
212
212
210
228a
228b
208
228b
228a
248a
206
248a
204
248b
218
218
202

Figure 7

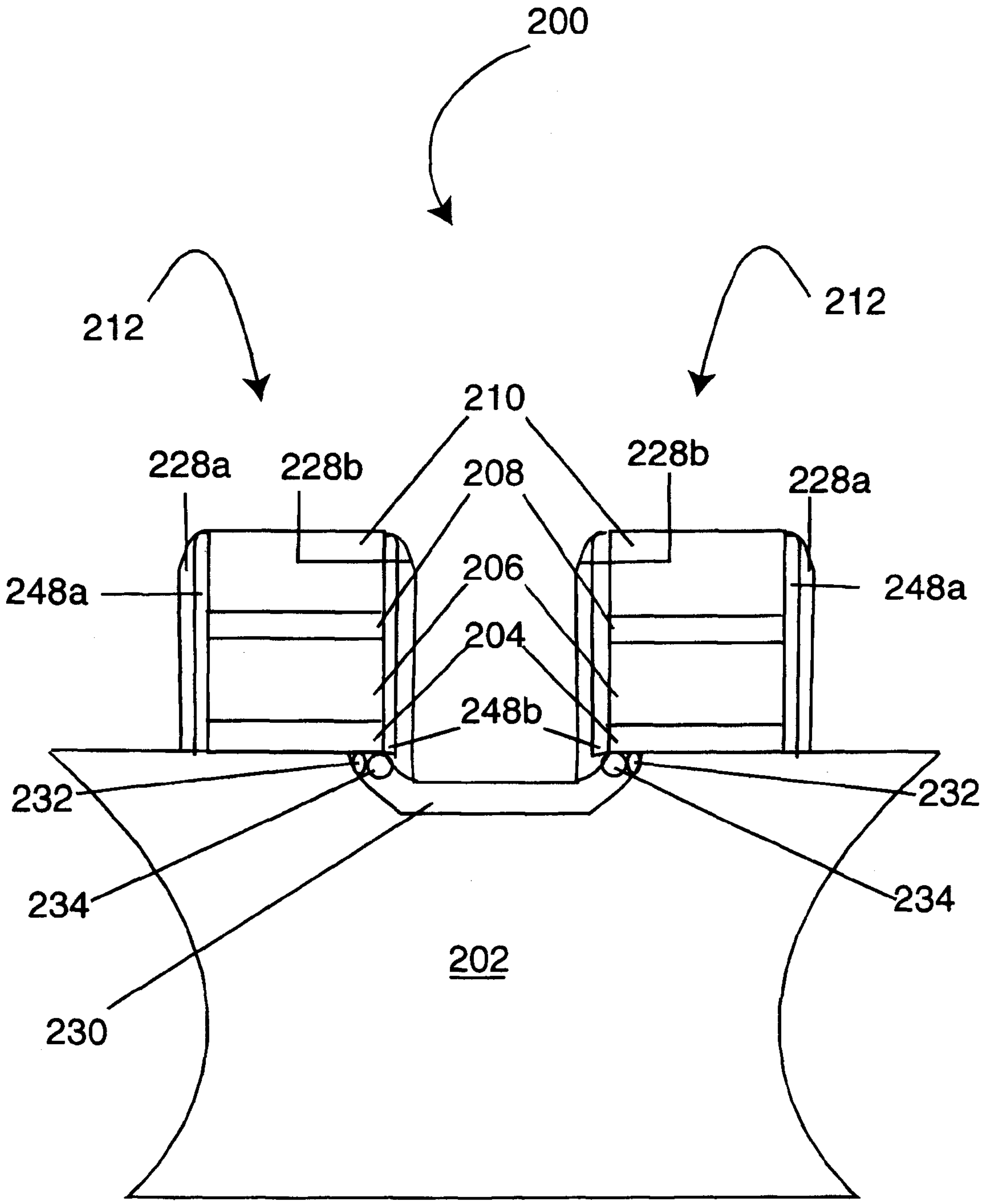

200
212
212
210
228a
228b
208
228b
228a
248a
206
248a
204
248b
232
232
234
234
202
230

Figure 8

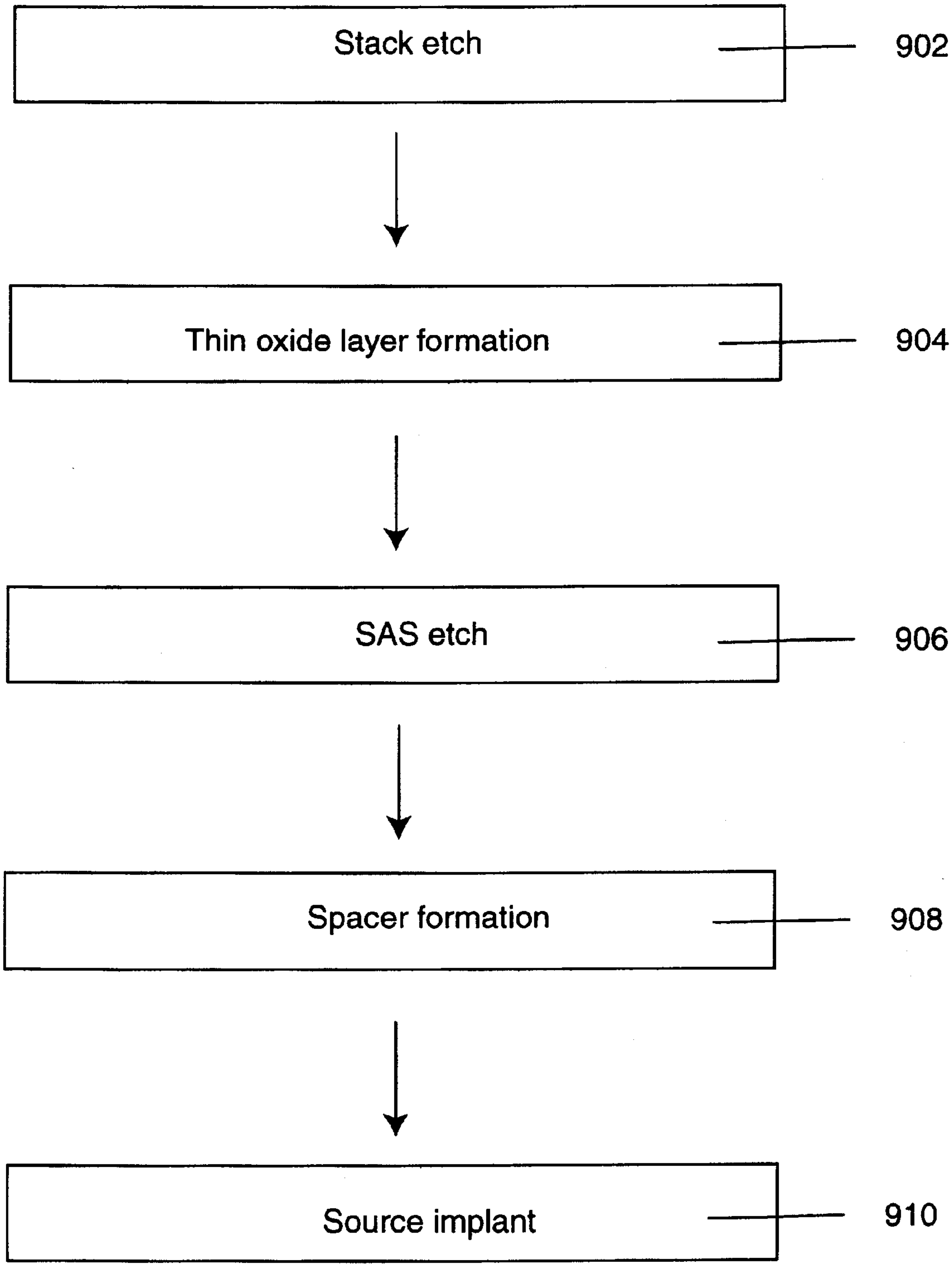

Stack etch
902
Thin oxide layer formation
904
SAS etch
906
Spacer formation
908
Source implant
910

Figure 9

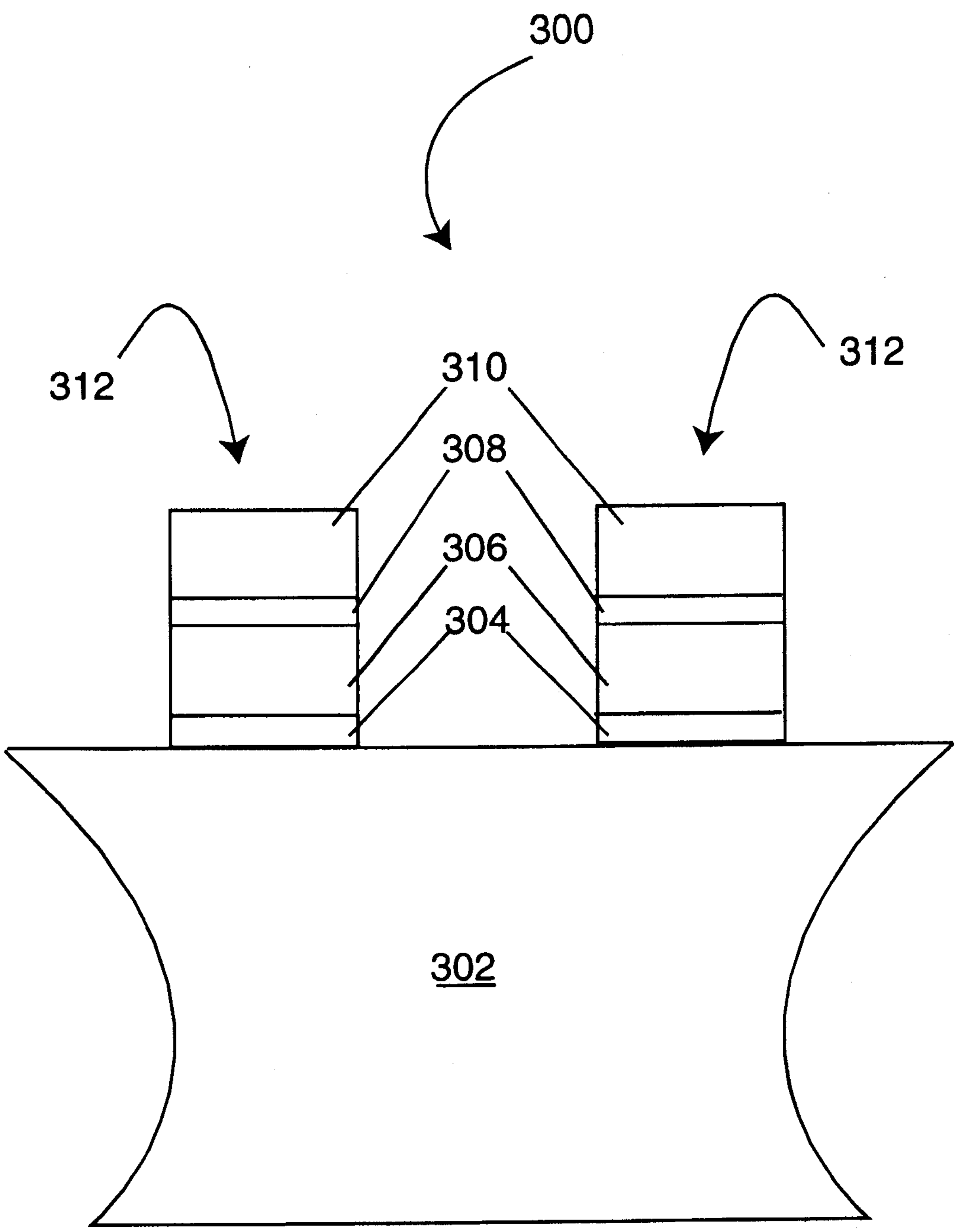


Figure 10

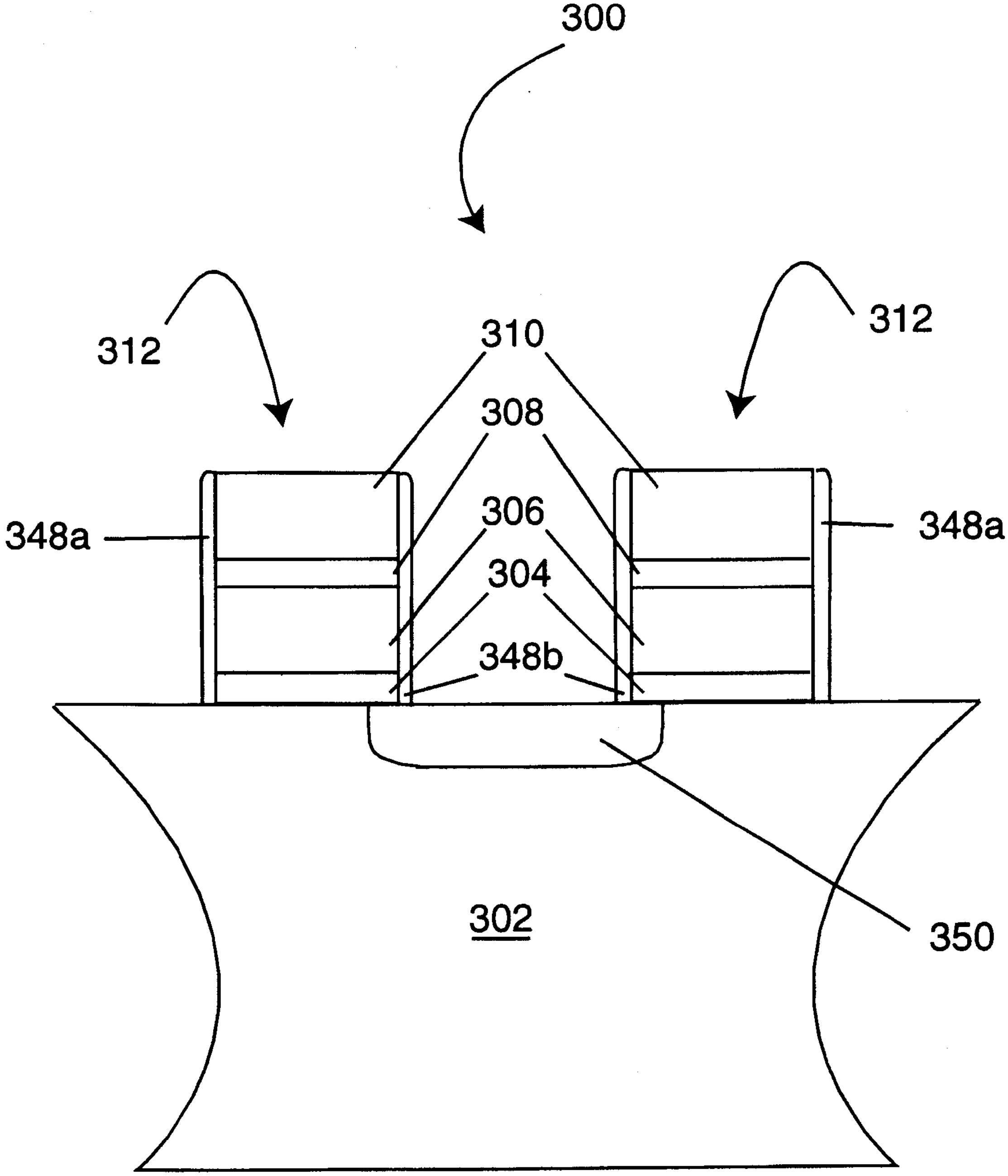


Figure 11

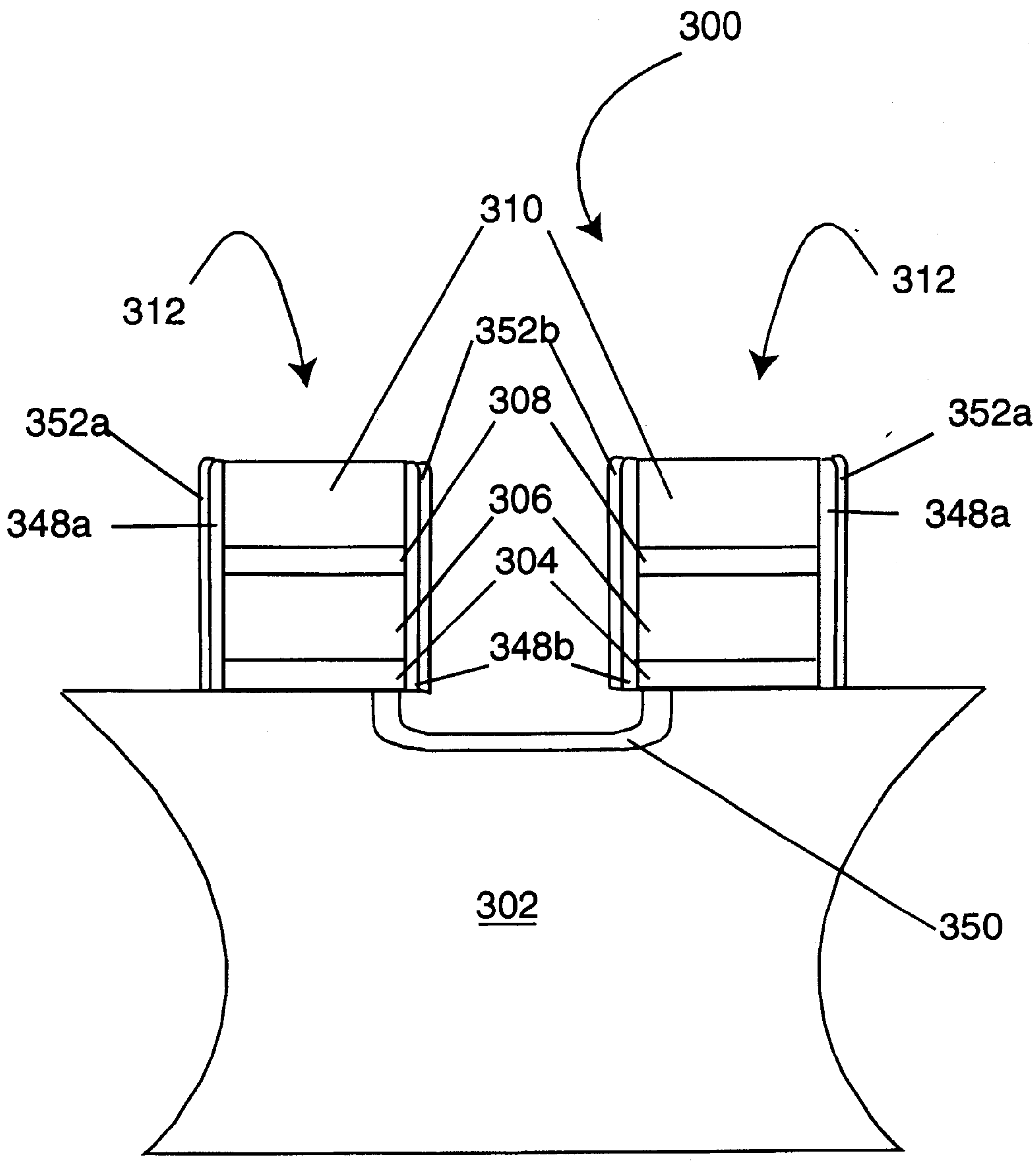

300
310
312
312
352b
308
352a
352a
348a
348a
306
304
348b
302
350

Figure 12

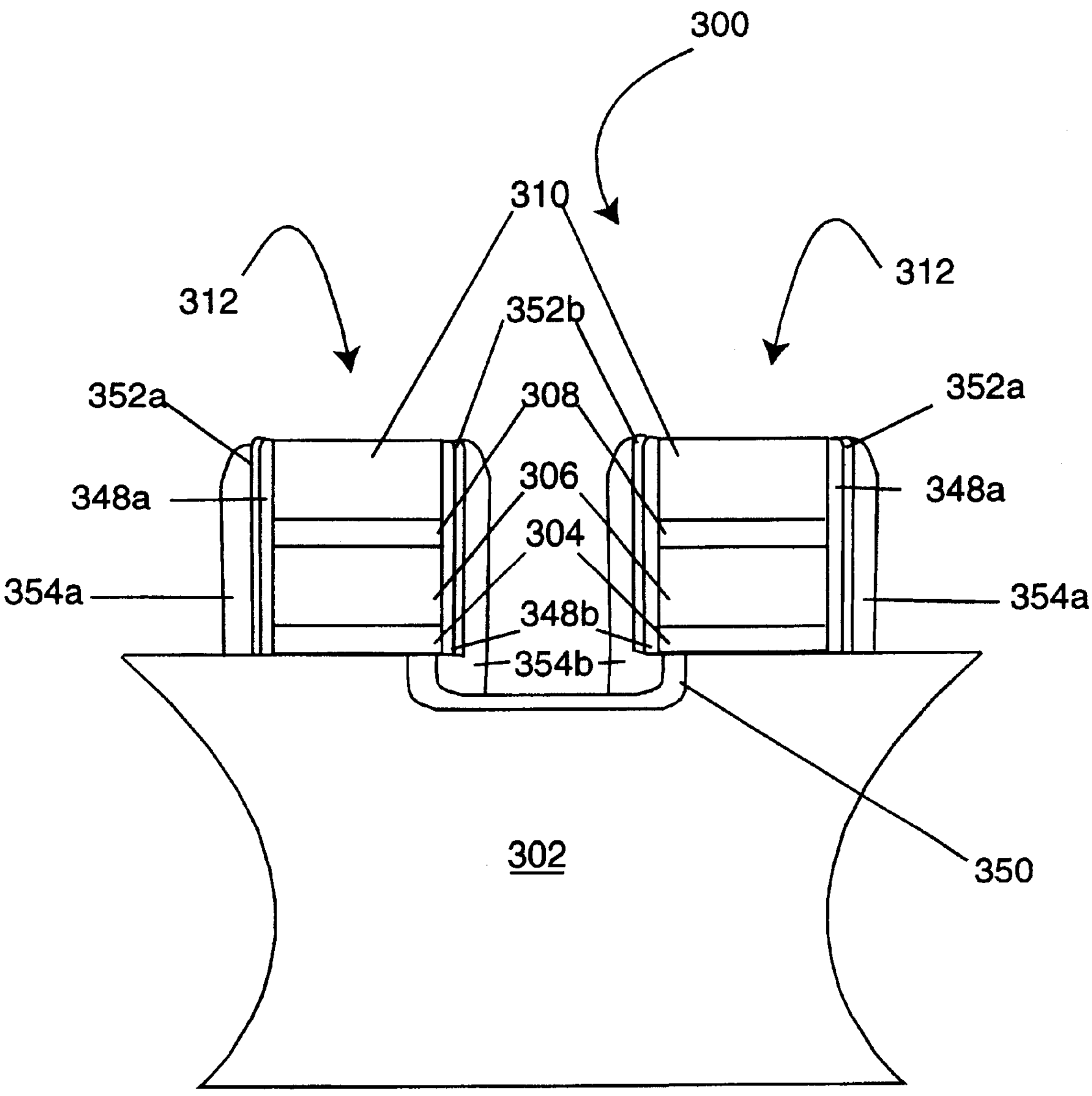

300
310
312
312
352b
352a
352a
308
348a
348a
306
304
354a
354a
348b
354b
302
350

Figure 13

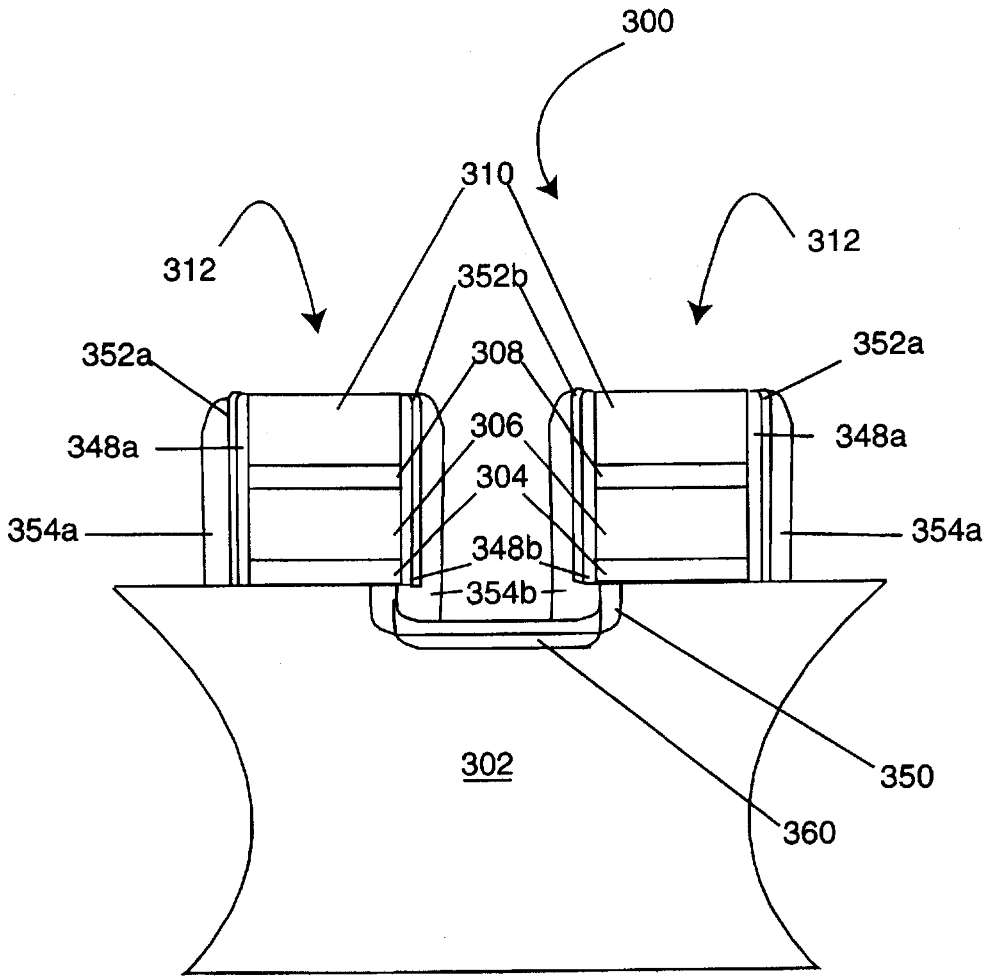


Figure 14A

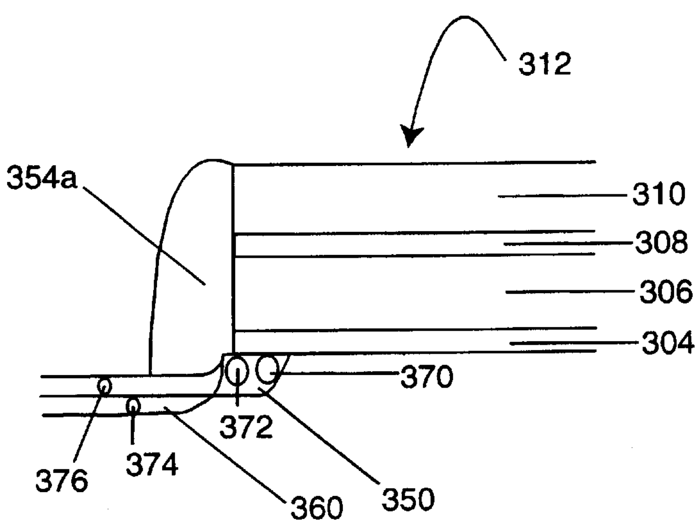


Figure 14B

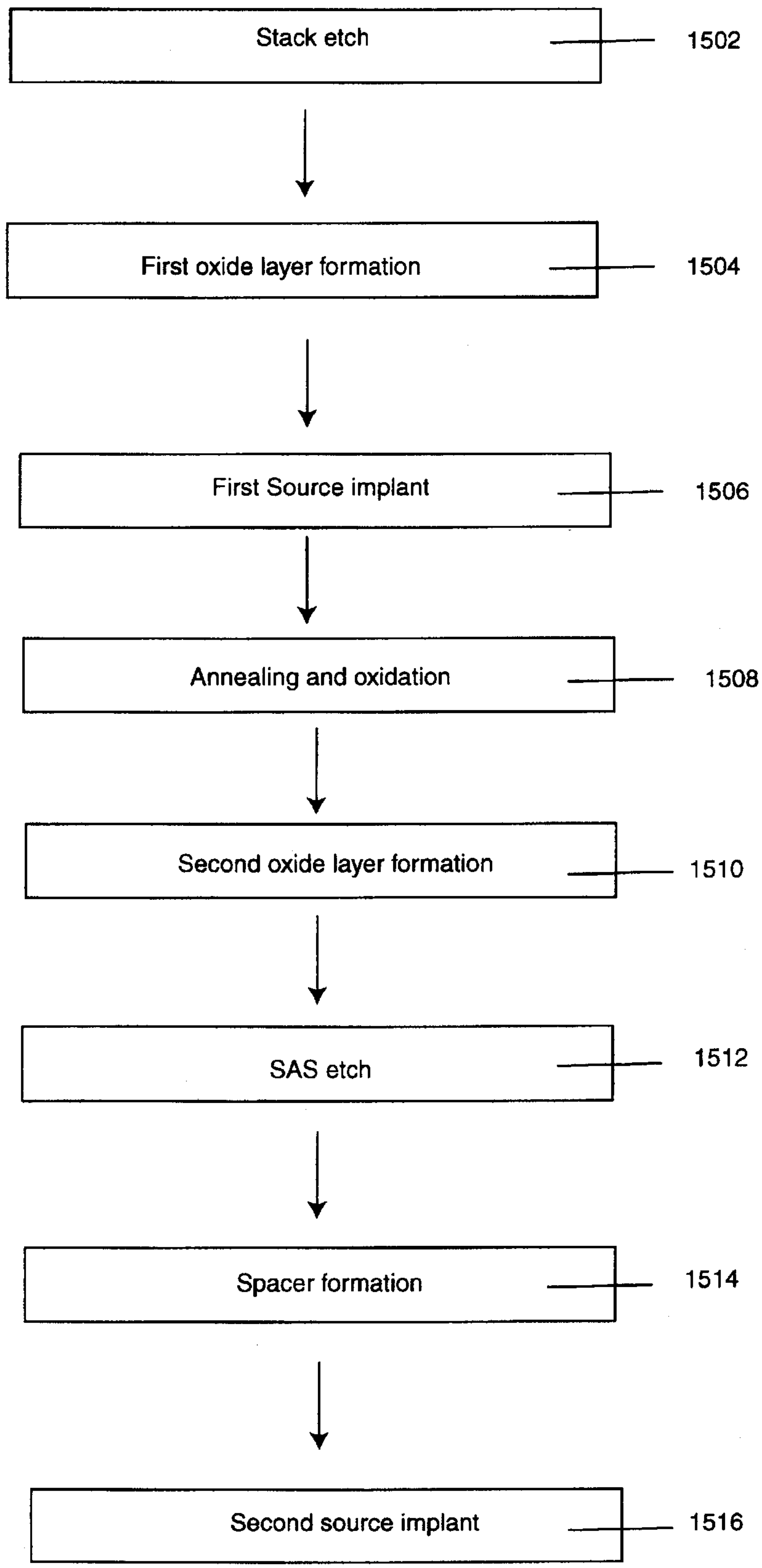

Stack etch
1502
First oxide layer formation
1504
First Source implant
1506
Annealing and oxidation
1508
Second oxide layer formation
1510
SAS etch
1512
Spacer formation
1514
Second source implant
1516

Figure 15

SEMICONDUCTOR DEVICE HAVING REDUCED SOURCE LEAKAGE DURING SOURCE ERASE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to flash EPROM cells and methods for their construction. More particularly, the current invention relates to reducing leakage during source erase of flash EPROM cells. More specifically, the present invention provides new process techniques that reduce source leakage during source erase of flash EPROM cells. The current invention also provides novel semiconductor devices with a differentially doped source region that reduces leakage during source erase.

2. Discussion of Related Art

Erasable programmable read-only memory (EPROM) is a form of non-volatile memory. Non-volatile memory devices retain information when power to the device is interrupted and thus are important in the design of wireless and portable electronic devices. Non-volatile storage choices range from mask read-only memory (ROM), ultraviolet EPROM (UV-EPROM), flash EPROM and electrically erasable EPROM (EEPROM).

EPROM devices typically lack the density of ROM disks but are more flexible since coded changes can be accommodated. EPROM devices offer the further advantage of rapid access since reading and writing to these types of devices is not delayed by the latency periods characteristic of ROM devices.

Flash EPROM offers some of the advantages of EEPROM with the lower cost of UV-EPROM. All forms of EPROM use electrical injection methods to program individual memory cells but differ in the method of memory cell erasure. Ultraviolet light irradiation is used to erase UV-EPROM memory cells. This method is non-selective and requires removal of memory cells from the system for erasure. EEPROM systems use Fowler-Nordheim tunneling to erase single cells which offers reprogramming flexibility, high density and convenience, since removal of memory cells from the device is not required for erasure.

Flash EPROM also uses Fowler-Nordheim tunneling for non-selective memory cell erasure. Thus, flash EPROM provides the convenience and high density of EEPROM with the low cost of conventional UV-EPROM. Therefore, flash EPROM has become the storage method of choice in many portable consumer devices such as cell phones and hand held personal computers.

Two different methods, which employ Fowler-Nordheim tunneling, are typically used to erase flash EPROM cells. In channel or substrate erase, a positive bias of about 10.0 V is applied to the substrate of the memory cell. Similarly, a negative bias of about −5.0 V is applied to the gate of the memory cell. Electron tunneling from the gate to the substrate then erases the memory cell. Channel erase requires source isolation by the triple well process, which is complicated and expensive.

Source erase is similar to substrate erase except that a positive bias of about 5.0 V is applied to the source of the memory cell while a negative bias of about −10.0 V is applied to the gate of the memory cell. Since source erase does not require source isolation by the triple well process it is simpler and less expensive to implement than channel erase.

However, a significant problem with source erase of flash EPROM cells is source diode leakage to the substrate during

erasure. Source leakage lengthens the time required to erase a flash EPROM and degrades performance. Source diode leakage must be minimized to increase source erase speed.

Three different mechanisms contribute to source diode leakage during source erase. Thermal leakage, which is intrinsic to any diode, is small and independent of electric field. Avalanche multiplication is electric field dependent and can become very large if the cell is not optimized during fabrication.

Band to band tunneling leakage is a fundamental problem with source erase (C. Chang et al., *Tech. Dig. IEDM,* 714, 1987; H. Kume et al., *Tech. Dig. IEDM,* 560, 1987). Band to band leakage wastes power since some of the diode current is dissipated in the substrate during erasure. Furthermore, constant source voltage is difficult to maintain in the presence of this type of leakage, which places significant demand on the charge pump capacitor. Thus, the difficulties caused by band to band leakage in generating and maintaining the voltage required to erase the device are frequently the limiting factor in source erasing flash cells.

The contour of the junction profile at the source edge under the stacked gate edge in flash EPROM cells strongly influences band to band tunneling. This may be best understood with reference to a prior art process typically used in the fabrication of flash EPROM cells, which is depicted in FIGS. 1–3.

FIG. **1** illustrates a partially fabricated semiconductor device **100** after stack etch. A pair of stacked gates **112** are disposed on a semiconductor substrate **102**. Stacked gates **112** are comprised of a tunnel oxide layer **104**, a first polysilicon layer **106**, an ONO layer **108** and a second polysilicon layer **110**. The partially fabricated semiconductor device **100** can be made by conventional methods known to one of skill in the semiconductor arts.

FIG. **2**A illustrates the partially fabricated semiconductor device of FIG. **1** after masking, self-aligned source (SAS) etch and mask removal (Tang et al., U.S. Pat. No. 5,120,671). These processing steps are conventional and are well known to one of skill in the semiconductor arts.

SAS etch connects source regions between adjacent cells after stacked gate formation. More specifically, SAS etch etches field oxide regions, which are used to isolate the active regions of flash EPROM cells. Consequently, the source region, formed between field oxide regions of adjacent memory cells, is self-aligned with both the polysilicon word line and the field oxide region. Self-alignment of the source region with the polysilicon word line and the field oxide region increases the density and reduces the cell size of a memory cell. Thus, SAS etch increases the performance and cost-effectiveness of flash EPROM cells.

A significant problem with SAS etch is over etching of the semiconductor substrate **102** at region **116**. Note that region **116** of the semiconductor substrate **102**, which was exposed to SAS etch, is not level with the stacked gate edge. Contrastingly, regions **115** of the semiconductor substrate which were not exposed to SAS etch are level with the stacked gate edge.

More importantly, the SAS etch creates a gouge in the semiconductor substrate at regions **118** in FIG. **2**A, which underlie the edge of stacked gates **112**. Furthermore, the integrity of tunnel oxide layer **104** is affected since the stacked gate edge is exposed to the SAS etch conditions. FIG. **2**B is an enlarged view of region **118**, which illustrates the damage caused by SAS etch. Note that a portion of tunnel oxide layer **104** is etched under layer **106**. The undercutting of semiconductor substrate **102** relative to the

stacked gate edge **120** significantly damages the tunnel oxide layer **104**. The ragged edge of the semiconductor substrate at **122** affects the uniformity of the subsequent ion implant to create the source region.

FIG. **3** illustrates the partially fabricated semiconductor device of FIG. **2** after SAS masking, source implantation, annealing and removal of the SAS mask. These conventional processing steps provide the source lines in a semiconductor device. Source region **124** has been formed under silicon surface **116**. However, since the edge of the source region under the stacked gate **112** was damaged during SAS etch the implant is not uniform. The non-uniform implant in source region **124** leads to non-uniform erase in the flash memory array which is caused by an insufficient dopant dose in the source overlap region with the stacked gates **112**. Furthermore, the non-uniform implant in source region **124** leads to excessive leakage caused by band to band tunneling, causing random failure in the array.

Nevertheless, it has become apparent that as flash EPROM cells shrink in size and increase in density that other methods of reducing source diode leakage are necessary. Thus, what is needed are efficient process methods that minimize band to band tunneling leakage caused by SAS etch.

SUMMARY OF THE INVENTION

The present invention addresses this need by providing new process methods that minimize source diode leakage. More specifically, the current invention reduces band to band tunneling leakage caused by SAS etch.

In one aspect, the current invention provides a method for reducing the source leakage of a semiconductor device. The method comprises providing a an etched stacked gate disposed on a semiconductor substrate, forming a thin oxide layer on the stacked gate, SAS etch, forming a spacer on the thin oxide layer and performing a source implant on the semiconductor substrate.

The thin oxide layer is formed by deposition and anisotropic etch of thin oxide. The SAS etch comprises the steps of SAS masking of the semiconductor device, field oxide etch and removing the SAS mask. The spacer may be formed by depositing a spacer layer and anisotropically etching the spacer layer. The source implant may be performed by SAS masking of the semiconductor device, implanting the source, annealing and removing the SAS mask. Preferably, the source implant is a phosphorus implant.

In one embodiment, the implanted source region has a first doped region disposed under the edge of the stacked gate and a second doped region disposed at the edge of the doped source region under the stacked gate. The second doped region has a higher concentration of dopant than the first doped region, which reduces source leakage of the semiconductor device. In a more specific embodiment, the second doped region has a dopant concentration of about 5×10^{19} atoms/cm^3 and the first doped region has a dopant concentration of about 1×10^{19} atoms/cm^3.

In another aspect, the current invention provides another method for reducing the source leakage of a semiconductor device. The method comprises providing an etched stacked gate disposed on a semiconductor substrate, forming a first oxide layer on the stacked gate, performing a first source implant, annealing, SAS etch, forming a second oxide layer on the first oxide layer, forming a spacer on the second oxide layer and performing a second source implant on the semiconductor substrate. Preferably, the first source implant is a phosphorus implant.

In one embodiment, the first oxide layer is between about 50 Å and about 100 Å. In another embodiment, the second oxide layer is between about 200 Å and about 500 Å.

In yet another aspect, the current invention provides a novel semiconductor device. The semiconductor device is comprised of a semiconductor substrate, a stacked gate provided on a portion of the semiconductor substrate, a first oxide layer provided on the edge of the stacked gate and a spacer provided on the first oxide layer. The semiconductor device also has a doped source region having a first doped region disposed under the edge of the stacked gate and a second doped region disposed at the edge of the doped source region under the stacked gate. The second doped region has a higher concentration of dopant than the first doped region, which reduces source leakage of the semiconductor device. Preferably, the doped source region is doped with phosphorus.

In one embodiment, the second doped region has a dopant concentration of about 5×10^{19} atoms/cm^3 and the first doped region has a dopant concentration of about 1×10^{19} atoms/cm^3. In another embodiment, the stacked gate is comprised of a tunnel oxide layer disposed on the semiconductor substrate, a first polysilicon layer disposed on the tunnel oxide layer, a ONO layer disposed on the first polysilicon layer and a second polysilicon layer disposed on the oxide layer. Preferably, the tunnel oxide layer is between about 60 Å and about 100 Å. In one embodiment, the first polysilicon layer is between about 500 Å and about 1500 Å. In another embodiment, the second polysilicon layer is between about 1000 Å and about 3000 Å. In yet another embodiment, the ONO layer is between about 120 Å and about 200 Å. Preferably, the channel length of the semiconductor device is between about 0.25 μm and about 0.50 μm.

In a final aspect, the current invention provides another novel semiconductor device. The semiconductor device is comprised of a semiconductor substrate, a stacked gate provided on a portion of the semiconductor substrate, a first oxide layer provided on the edge of the stacked gate, a second oxide layer provided on the first oxide layer and a spacer provided on the second oxide layer. The semiconductor device also has a doped source region having a first doped region disposed under the edge of the stacked gate and a second doped region disposed at the edge of the doped source region under the stacked gate. The second doped region has a higher concentration of dopant than the first doped region, which reduces source leakage of the semiconductor device. Preferably, the doped source region is doped with phosphorus.

In one embodiment, the second doped region has a dopant concentration of about 5×10^{19} atoms/cm^3 and the first doped region has a dopant concentration of about 1×10^{19} atoms/cm^3. In another embodiment, the stacked gate is comprised of a tunnel oxide layer disposed on the semiconductor substrate, a first polysilicon layer disposed on the tunnel oxide layer, a ONO layer disposed on the first polysilicon layer and a second polysilicon layer disposed on the oxide layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the following description taken in conjunction with the accompanying drawings in which:

FIG. **1** illustrates a partially fabricated semiconductor device after stack etch;

FIG. **2A** illustrates the partially fabricated semiconductor device of FIG. **1** after SAS masking, SAS etch and SAS mask removal;

FIG. 2B illustrates an enlarged view of region **118** depicted in FIG. **2A**;

FIG. **3** illustrates the partially fabricated semiconductor device of FIG. **2A** after SAS masking, source implantation, annealing and SAS mask removal;

FIG. **4** illustrates a partially fabricated semiconductor device;

FIG. **5** illustrates the partially fabricated semiconductor device of FIG. **4** after SAS etch;

FIG. **6** illustrates the partially fabricated semiconductor device of FIG. **5** after blanket deposition of spacer oxide layer;

FIG. **7** illustrates the partially fabricated semiconductor device of FIG. **6** after spacer etch;

FIG. **8** illustrates the partially fabricated semiconductor device of FIG. **7** after SAS masking, source implant, annealing and SAS mask removal;

FIG. **9** summarizes the process sequence of a first embodiment of the present invention;

FIG. **10** illustrates a partially fabricated semiconductor device;

FIG. **11** illustrates the partially fabricated semiconductor device of FIG. **10** after SAS masking, a first source implant, SAS mask removal, annealing and oxidation, blanket deposition of a first oxide layer and oxide etch;

FIG. **12** illustrates the partially fabricated semiconductor device of FIG. **11** after growth of a second oxide layer on the first oxide layer, SAS masking, SAS etch and SAS mask removal;

FIG. **13** illustrates the partially fabricated semiconductor device of FIG. **12** after blanket deposition of spacer and spacer etch;

FIG. **14A** illustrates the partially fabricated semiconductor device of FIG. **13** after SAS masking, a second source implant and SAS mask removal;

FIG. **14B** illustrates an enlarged view of stacked gate edge and source implant regions depicted in FIG. **14A**; and

FIG. **15** summarizes the process sequence of a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the invention. Examples of preferred embodiments are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that it is not intended to limit the invention to those preferred embodiments. To the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

One embodiment of the current invention begins with the partially fabricated semiconductor device **200** shown in FIG. **4**. Stacked gates **212**, formed by stack etch under conventional conditions, are disposed on semiconductor substrate **202**. In one embodiment, the semiconductor substrate **202** is a uniformly lightly p-doped single crystal silicon wafer. The channel length of the partially fabricated semiconductor device may be between about 0.25 μm and about 0.50 μm. Stacked gates **212** are comprised of a tunnel oxide layer **204**, a first polysilicon layer **206**, an ONO layer **208** and a second polysilicon layer **210**. In the described embodiment, the tunnel oxide layer may be between 60 Å and about 100 Å,

the first polysilicon layer may be between about 500 Å and about 1500 Å, the ONO layer may be between about 120 Å and about 200 Å and the second polysilicon layer may be between about 1000 Å and about 3000 Å.

Thin oxide layers **248*a*** and **248*b***, which are appended to the edges of stacked gates **212**, are formed after stack etch by deposition and anisotropic etch of thin oxide. In the described embodiment, thin oxide layers **248*a*** and **248*b*** may be between about 100 Å and about 500 Å. The thin oxide layer ensures good sidewall sealing for the ONO layer **208** and tunnel oxide layer **204**. The thin oxide layer is sometimes called the seal oxide.

As illustrated in FIG. **5**, the partially fabricated semiconductor substrate **200** has been subjected to SAS etch. Note that region **216**, which was exposed to SAS etch, is not level with the stacked gate edge. More importantly, the SAS etch has gouged the semiconductor substrate at regions **218** in FIG. **4**, which are adjacent to the edge of stacked gates **212**.

As shown in FIG. **6** a spacer oxide layer **226** is then deposited. Conventional methods well known in the art may be used to deposit spacer oxide layer **226**. In the described embodiment, the spacer oxide layer may be between about 500 Å and about 1500 Å.

Anisotropic spacer etch, performed, for example, with conventional reactive ion etching (RIE), provides the partially fabricated semiconductor device shown in FIG. **7**. Spacers **228*a*** and **228*b*** have been formed on the thin oxide layers **248*a*** and **248*b***, which adhere to the sides of stacked gates **212**. In the described embodiment, spacers **228*a*** and **228*b*** are between about 500 Å and about 1500 Å. Importantly, spacers **228*b*** cover the gouged regions of the semiconductor substrate **218**, the oxide layers **248*a*** and **248*b*** and the stacked gate edges. The presence of spacers **228*a*** and **228*b*** on the stacked gates significantly improves the uniformity of the subsequent source implant step, which reduces band to band tunneling leakage in source erase.

FIG. **8** illustrates partially fabricated semiconductor device **200** after SAS mask formation, source implant in the semiconductor substrate, annealing and removal of the SAS mask. SAS mask formation and removal are conventional steps well known in the art. In the described embodiment, the device is implanted with n-type dopant at various dosages ranging from between about 10^{14} ions/cm^2 to about 5×10^{15}/cm^2 (more preferably between about 5×10^{14} ions/cm^2 to about 10^{15} ions/cm^2) at energies ranging from about 30 keV to about 60 keV (preferably about 30 keV) using conventional ion implantation equipment. In one embodiment, a tilted implant method is used to implant the source, which has the advantage of increasing the amount of implant diffusion under the sidewalls. Typically, the annealing step is performed between about 800° C. and about 1000° C. Preferably, the annealing step is performed at about 900° C.

Preferably, the implant is a phosphorus implant without any arsenic. Phosphorus implants are known to create fewer defects than arsenic within the crystal, which reduces source diode leakage.

The implanted semiconductor device depicted in FIG. **8** has source region **230** that has at least two doped regions **232** and **234** that differ in dopant concentration. The SAS line (also referred to as the source line) created by the implant has been displaced slightly relative to the stacked gates **212**. More importantly, the SAS implant is self-aligned to the spacer and not the stacked gate edge. This is a significant advantage over the conventional process where the roughness of the stacked gate edge leads to non-uniform implant,

which causes band to band tunneling leakage. The smooth surface of the spacer leads to a more uniform implant and consequently a superior junction profile.

Importantly, the present invention relies on diffusion of the implant under the spacer sidewalls to create two doped regions **232** and **234** in source region **230**, which differ in dopant concentration. Region **234** is under the edge of stacked gates **212**. Region **232** is adjacent to region **234** and is at the edge of source region **230** under stacked gates **212**. Typically, the dopant concentration in region **232** is greater than the dopant concentration in region **234**. In one embodiment, the dopant concentration in region **234** is about 1×10^{19} atom/cm^3 while the dopant concentration in region **232** is about 5×10^{19} atom/cm^3. Heavily doped region **232**, which is displaced away from the stacked gate edge, directs electron flow to the stacked gate. Thus, leakage caused by the high field at the gate edge is reduced since electron flow is channeled through region **232**, where the field is slightly lower and which is less damaged by stack gate etch and SAS etch.

The described process sequence is summarized in FIG. **9**. A partially fabricated semiconductor device made by methods well known to those of skill in the art is subjected to conventional stack etch at **902**. A thin oxide layer is attached to the sides of the stacked gate at **904** by thin oxide deposition and anisotropic etch. SAS etch at **906**, followed by spacer formation at **908** and source implant at **910** provides the partially fabricated semiconductor device illustrated FIG. **8**.

The embodiment described above possesses a number of advantages over the prior art. First, because the implant is performed after spacer formation, a smoother junction is formed. Second, a more uniform implant is observed because the implant is self-aligned to the spacer rather than the gouged stack edge. Third, a region of high dopant concentration is located away from the stacked gate edge which was significantly damaged by SAS etch. Fourth, the implant may be a phosphorus implant that reduces crystal defects. The culmative effect of these aforementioned advantages is to provide a semiconductor device with reduced levels of leakage during source erase.

A second embodiment of the current invention begins with the partially fabricated semiconductor device **300** shown in FIG. **10**. Stacked gates **312**, disposed on semiconductor substrate **302** are formed by conventional stack etch. In one embodiment, the semiconductor substrate **302** may be a uniformly lightly p-doped single crystal silicon wafer. The channel length of the partially fabricated semiconductor device may be between about 0.25 μm and about 0.50 μm. Stacked gates **312** are comprised of a tunnel oxide layer **304**, a first polysilicon layer **306**, an ONO layer **308** and a second polysilicon layer **310**. In the described embodiment, the tunnel oxide layer may be between 60 Å and about 100 Å, the first polysilicon layer may be between about 500 Å and about 1500 Å, the ONO layer may be between about 120 Å and about 200 Å and the second polysilicon layer may be between about 1000 Å and about 3000 Å.

The following sequence of process steps provides the partially fabricated semiconductor device shown in FIG. **11** from the structure depicted in FIG. **10**: SAS masking, a first source implant, annealing and oxidation, SAS mask removal, deposition of a first oxide layer and anisotropic etch of the first oxide layer. First oxide layers **348*a*** and **348*b*** have been appended to the edges of stacked gates **312** and source region **350** has been formed. Source region **350** is preferably implanted with phosphorus.

In one embodiment, the first source implant is preferably phosphorus at various dosages ranging from between about 10^{14} ions/cm^2 to about 5×10^{15} ions/cm^2 (more preferably between about 10^{15} ions/cm^2 to about 2×10^{15} ions/cm^2) at energies ranging from about 40 keV to about 60 keV (preferably about 50 keV) using conventional ion implantation equipment. Typically, the annealing step is performed between about 800° C. and about 1000° C. Preferably, the annealing step is performed at about 900° C.

In the described embodiment, the first oxide layer may be between 100 Å and about 500 Å. The first oxide layer ensures good sidewall sealing for the ONO layer **308** and tunnel oxide layer **304**. The first oxide layer is sometimes called the seal oxide.

Growth of second oxide layers **352*a*** and **352*b*** on first oxide layers **348*a*** and **348*b*** followed by the conventional process sequence of SAS masking, SAS etch and mask removal provides the partially fabricated semiconductor device shown in FIG. **12**. In one embodiment, the second oxide layer may be between 50 Å and about 100 Å. The second oxide layer reduces the damage to the tunnel oxide since the first oxide layer may not sufficiently protect layer **304** during SAS etch. Note that the top portion of source region **350** has been removed by SAS etch which negatively affects subsequent performance.

FIG. **13** illustrates the partially fabricated semiconductor device of FIG. **12** after spacer deposition and anisotropic etch of the spacer layer. Note that spacer layers **354*a*** and **354*b*** have been formed on top of second oxide layers **352*a*** and **352*b*** on the edge of stacked gates **312**. In the exemplified embodiment, the spacer may be between about 500 Å and about 1500 Å.

The sequential steps of SAS masking, source implant and SAS mask removal provide the structure illustrated in FIG. **14**A. In one embodiment, the source implant may be a n-type dopant (preferably phosphorus) at various dosages ranging from between about 10^{15} ions/cm^2 to about 10^{16}/cm^2 (more preferably between about 3×10^{15} ions/cm^2 to about 5×10^{15} ions/cm^2) at energies ranging from about 30 keV to about 60 keV (preferably about 40 keV) using conventional ion implantation equipment. The source implant forms a second source region **360** which overlaps the first source region **350**.

FIG. **14**B illustrates an enlarged view of the stacked gate edge and source implant regions depicted in FIG. **14**A. Oxide layers **352** and **348** are not shown on the edge of stacked gate **312** for the sake of clarity. The first source implant region **350** and the second source implant region **360** are located below the spacer **354** and the edge of the stacked gate.

Region **370** at the edge of source implant region **350** under the stacked gate has a dopant concentration of between about 5×10^{19} atoms/cm^3 and about 1×10^{20} atoms/cm^3. Region **372** directly under the edge of the stacked gate in source implant area **350** has a dopant concentration of between about 10^{19} atoms/cm^3 and about 5×10^{19} atoms/cm^3. Region **374** in source region **360** has a dopant concentration of between about 10^{18} atoms/cm^3 and about 10^{19} atoms/cm^3. Finally, region **376** in source region **370** has a dopant concentration of between about 10^{20} atoms/cm^3 and about 5×10^{20} atoms/cm^3. It should be understood that the dopant concentration in regions **370, 372, 374** and **376** might differ from the values provided above. However, the dopant concentration pattern using the method of the current invention will approximate the dopant distribution shown in FIG. **14**B.

Heavily doped region **370**, which is displaced away from the stacked gate edge, directs electron flow to the stacked gate. Thus, leakage caused by the high field at the gate edge is reduced since electron flow is channeled through region **370**, where the field is slightly lower and which is less damaged by stack gate etch and SAS etch.

The described process sequence is summarized in FIG. **15**. A partially fabricated semiconductor device, made by methods well known to those of skill in the art, is subjected to conventional stack etch at **1502**. A first oxide layer is attached to the sides of the stacked gate at **1504** by first oxide deposition and anisotropic etch. A first source implant is performed at **1506** followed by annealing and oxidation at **1508**. Formation of a second oxide layer at **1510**, followed by SAS etch at **1512** and spacer formation at **1514** and a second source implant at **1516** provides the partially fabricated semiconductor device illustrated in FIG. **14A**.

The described embodiment has some significant advantages over the prior art. Because the first source implant is performed before SAS etch and the second source implant is performed after spacer formation, a smoother junction is formed under the stacked gate. Second, a more uniform implant is observed because the second source implant is self aligned to the spacer rather than the gouged stack edge. Preferably, the first source implant is a phosphorus implant which causes less crystal defects. The region of high dopant concentration **370** under the stacked gate is located away from the stacked gate edge which is damaged by SAS etch. These aforementioned advantages provide a semiconductor device with reduced levels of leakage during source erase.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims.

Furthermore, it should be noted that there are alternative ways of implementing both the process and apparatus of the present invention. For example, the semiconductor substrate may be a lightly doped n-type silicon wafer. The semiconductor device may then be implanted with a p-type dopant. The source regions adjacent to the stacked gate may have different dopant concentrations than those mentioned in the described embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

1. A semiconductor device comprising:

a stacked gate provided on a portion of a semiconductor substrate;

a first oxide layer provided on the edge of the stacked gate;

a spacer provided adjacent the first oxide layer; and

a doped source region, the source region having a first doped region disposed under the edge of the stacked gate and a second doped region disposed at the edge of the doped source region under the stacked gate;

wherein the second doped region has a higher concentration of dopant than the first doped region, whereby source leakage of the semiconductor device is reduced.

2. The semiconductor device of claim **1**, wherein the second doped region has a dopant concentration of about

10^{20} atoms/cm^3 and the first doped region has a dopant concentration of about 5×10^{19} atoms/cm^3.

3. The semiconductor device of claim **1**, wherein the stacked gate comprises:

a tunnel oxide layer disposed on the semiconductor substrate;

a first polysilicon layer disposed on the tunnel oxide layer;

a ONO layer disposed on the first polysilicon layer; and

a second polysilicon layer disposed on the ONO layer.

4. The semiconductor device of claim **3**, wherein the tunnel oxide layer is between about 60 Å and about 100 Å.

5. The semiconductor device of claim **3**, wherein the first polysilicon layer is between about 500 Å and about 1500 Å.

6. The semiconductor device of claim **3**, wherein the second polysilicon layer is between about 1000 Å and about 3000 Å.

7. The semiconductor device of claim **3**, wherein the ONO layer is between about 120 Å and about 200 Å.

8. The semiconductor device of claim **1**, wherein the first oxide layer is between about 100 Å and about 500 Å.

9. The semiconductor device of claim **1**, wherein the channel length of the semiconductor device is between about 0.25 μm and about 0.50 μm.

10. The semiconductor device of claim **1**, wherein the spacer is between about 500 Å and about 1500 Å.

11. The semiconductor device of claim **1** wherein the doped source region is doped with phosphorus.

12. A semiconductor device comprising:

a stacked gate provided on a portion of a semiconductor substrate;

a first oxide layer provided on the edge of the stacked gate;

a second oxide layer provided adjacent the first oxide layer;

a spacer provided adjacent the second oxide layer; and

a doped source region, the source region having a first doped region disposed under the edge of the stacked gate and a second doped region disposed at the edge of the doped source region under the stacked gate;

wherein the second doped region has a higher concentration of dopant than the first doped region, whereby source leakage of the semiconductor device is reduced.

13. The semiconductor device of claim **12**, wherein the second doped region has a dopant concentration of about 5×10^{19} atoms/cm^3 and the first doped region has a dopant concentration of about 1×10^{19} atoms/cm^3.

14. The semiconductor device of claim **12**, wherein the stacked gate comprises:

a tunnel oxide layer disposed on the semiconductor substrate;

a first polysilicon layer disposed on the tunnel oxide layer;

a ONO layer disposed on the first polysilicon layer; and

a second polysilicon layer disposed on the ONO layer.

15. The semiconductor device of claim **12**, wherein the channel length of the semiconductor device is between about 0.25 μm and about 0.50 μm.

16. The semiconductor device of claim **12**, wherein the doped source region is doped with phosphorus.

17. The semiconductor device of claim **12**, wherein the second oxide layer is between about 50 Å and about 100 Å.

* * * * *

CIVIL COVER SHEET

3-08CV0977-M

The JS-44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON THE REVERSE OF THE FORM.)

I. (a) PLAINTIFFS
FAST MEMORY ERASE, LLC

DEFENDANT:
SPANSION, INC. *et al.*,

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CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF TEXAS

(b) COUNTY OF RESIDENCE OF FIRST LISTED PLAINTIFF Dallas County, Texas
(EXCEPT IN U.S. PLAINTIFF CASES)

COUNTY OF RESIDENCE OF FIRST LISTED DEFENDANT Santa Clara County, California
(IN U.S. PLAINTIFF CASES ONLY)
NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE TRACT OF LAND INVOLVED.

(c) ATTORNEYS (FIRM NAME, ADDRESS, AND TELEPHONE NUMBER)
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325 N. St. Paul Street, Suite 4450
Dallas, Texas 75201 (214) 593-9110

ATTORNEYS (IF KNOWN)
UNKNOWN

II. BASIS OF JURISDICTION (PLACE AN "X" IN ONE BOX ONLY)

- ☐ **1 U.S. Government Plaintiff**
- ☒ **3 Federal Question (U.S. Government Not a Party)**
- ☐ **2 U.S. Government Defendant**
- ☐ **4 Diversity (Indicate Citizenship of Parties in Item III)**

III. CITIZENSHIP OF PRINCIPAL PARTIES (PLACE AN "X" IN ONE BOX FOR PLAINTIFF AND ONE BOX FOR DEFENDANT)
(For Diversity Cases Only)

	PTF	DEF		PTF	DEF
Citizenship of This State	☐ 1	☐ 1	**Incorporated *or* Principal Place of Business In This State**	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	**Incorporated *and* Principal Place of Business In Another State**	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	**Foreign Nation**	☐ 6	☐ 6

IV. NATURE OF SUIT (*PLACE AN "X" IN ONE BOX ONLY*)

CONTRACT
- ☐ 110 Insurance
- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment & Enforcement of Judgment
- ☐ 151 Medicare Act
- ☐ 152 Recovery of Defaulted Student Loans (Excl. Veterans)
- ☐ 153 Recovery of Overpayment of Veteran's Benefits
- ☐ 160 Stockholders' Suits
- ☐ 190 Other Contract
- ☐ 195 Contract Product Liability

REAL PROPERTY
- ☐ 210 Land Condemnation
- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment
- ☐ 240 Torts to Land
- ☐ 245 Tort Product Liability
- ☐ 290 All Other Real Property

TORTS

PERSONAL INJURY
- ☐ 310 Airplane
- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel & Slander
- ☐ 330 Federal Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Product Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury

PERSONAL INJURY
- ☐ 362 Personal Injury-Med. Malpractice
- ☐ 365 Personal Injury-Product Liability
- ☐ 368 Asbestos Personal Injury Product Liability

PERSONAL PROPERTY
- ☐ 370 Other Fraud
- ☐ 371 Truth in Lending
- ☐ 380 Other Personal Property Damage
- ☐ 385 Property Damage Product Liability

CIVIL RIGHTS
- ☐ 441 Voting
- ☐ 442 Employment
- ☐ 443 Housing/Accommodations
- ☐ 444 Welfare
- ☐ 440 Other Civil Rights

PRISONER PETITIONS
- ☐ 510 Motions to Vacate Sentence Habeus Corpus:
- ☐ 530 General
- ☐ 535 Death Penalty
- ☐ 540 Mandamus & Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition

FORFEITURE/PENALTY
- ☐ 610 Agriculture
- ☐ 620 Other Food & Drug
- ☐ 625 Drug Related Seizure of Property 21 USC 881
- ☐ 630 Liquor Laws
- ☐ 640 R.R. & Truck
- ☐ 650 Airline Regs.
- ☐ 660 Occupational Safety/Health
- ☐ 690 Other

LABOR
- ☐ 710 Fair Labor Standards Act
- ☐ 720 Labor/Mgmt Relations
- ☐ 730 Labor/Mgmt. Reporting & Disclosure Act
- ☐ 740 Railway Labor Act
- ☐ 790 Other Labor Litigation
- ☐ 791 Empl. Ret. Inc. Security Act

BANKRUPTCY
- ☐ 422 Appeal 28 USC 158
- ☐ 423 Withdrawal 28 USC 157

PROPERTY RIGHTS
- ☐ 820 Copyrights
- ☒ 830 Patent
- ☐ 840 Trademark

SOCIAL SECURITY
- ☐ 861 HIA (1395ff)
- ☐ 862 Black Lung (923)
- ☐ 863 DIWC/DIWW (405(g))
- ☐ 864 SSID Title XVI
- ☐ 865 RSI (405(g))

FEDERAL TAX SUITS
- ☐ 870 Taxes (U.S. Plaintiff or Defendant)
- ☐ 871 IRS - Third Party 26 USC 7609

OTHER STATUTES
- ☐ 400 State Reapportionment
- ☐ 410 Antitrust
- ☐ 430 Banks and Banking
- ☐ 450 Commerce/ICC Rates/etc.
- ☐ 460 Deportation
- ☐ 470 Racketeer Influenced and Corrupt Organizations
- ☐ 810 Selective Service
- ☐ 850 Securities/Commodities/Exchange
- ☐ 875 Customer Challenge 12 USC 3410
- ☐ 891 Agricultural Acts
- ☐ 892 Economic Stabilization Act
- ☐ 893 Environmental Matters
- ☐ 894 Energy Allocation Act
- ☐ 895 Freedom of Information Act
- ☐ 900 Appeal of Fee Determination Under Equal Access to Justice
- ☐ 950 Constitutionality of State Statutes
- ☐ 890 Other Statutory Actions

V. ORIGIN (*PLACE AN "X" IN ONE BOX ONLY*)

☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify) ☐ 6 Multidistrict Litigation ☐ 7 Appeal to District Judge from Magistrate Judge

VI. CAUSE OF ACTION (Cite the U.S. Civil Statute under which you are filing and write brief statement of cause. Do not cite jurisdictional statutes unless diversity.)
Action under 28 U.S.C. § 1331, 28 U.S.C. § 1338, and 35 U.S.C. § 271 *et seq.*, for patent infringement

VII. REQUESTED IN COMPLAINT: ☐ CHECK IF THIS IS A **CLASS ACTION** UNDER F.R.C.P. 23
DEMAND $ unspecified
CHECK YES only if demanded in complaint:
JURY DEMAND: ☒ YES ☐ NO

VIII. RELATED CASE(S) IF ANY (See instructions): JUDGE DOCKET NUMBER

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